Joint Symposium eMDC-2017 & ISSM-2017

Keynote Speech: Heterogeneous Integration in Silicon Age 4.0 Delivering Intelligences for VR/AR, Robotics and AI

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About the Speaker

- As a researcher, design architect and chief executive, Dr. Lu has dedicated his career to the worldwide IC design and semiconductor industry
- A Serial Entrepreneur to Create/Co-Lead Several Successful Semiconductor Companies (Etron, Ardentec Corp., Global Unichip Corp., etc.) Translating Technology Innovations to Real-World Impact and Economic Successes
- Chairman (2013-17) & Board Director (1998-Now) of TSIA (Taiwan Semiconductor Industry Association)
- Chairman (2014-2015) of WSC (World Semiconductor Council)
- Chairman(2009-11) and Board Director (2004-Now) of GSA (Global Semiconductor Alliance)
- BSEE, National Taiwan U., MSEE/PhD, Stanford U.; Authored over 60 papers & 30 US Patents
- Member, National Academy of Engineering of USA; IEEE Fellow; IEEE 1998 Solid-State Circuits Award Recipient; Scientific Management Award (2012), Chinese Society for Management of Technology; Golden Merchant Award (2007), General Chamber of Commerce of R.O.C.
- Distinguished Alumnus, National Chiao-Tung University (1998) & National Taiwan University (2011), Respectively; Associate Professor & Chair Professor, National Chiao-Tung University (1981-1982 & 2005-2008)
- Invented/Realized the Most Dense SPT Trench DRAM Cell (1985) and Designed the World's Fastest High-Speed DRAM Chip(1987) in IBM Research and as Program Manager in IBM Headquarters; Received the Corporate Highest-Honor Award (1990)
- Recipient of the 2001 National Medal of Excellence in Science & Technology in Taiwan for Pioneering National Submicron Project's 8"-wafer advanced Technology, IC Designs and Architected a Fabless-Foundry-Subsystem Infrastructure in Taiwan

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Abstract

Over the last five decades, the semiconductor industry has grown tremendously, from its infancy to now reaching over US$350 billion in annual revenue. This growth has been underpinned by two intelligent rules: one is an effective Return-on-Investment economic rule based on Moore's Law, which dictates that the number of transistors on a silicon chip should double every two years. The other rule is a design guideline, namely, scaling transistor line width to achieve enough productivity in lower power-delay products. Now that the line width has shrunk from several micrometers to 10 nanometers, the critical question the integrated-circuit industry faces is how far can both rules sustain? This talk proposes two points: firstly, a new observation on how the industry can continue to be very efficient and keep Moore's Law effectively for the 10 nanometer technology node. Secondly, this talk makes a bold prediction that we will see a new guideline, which can be called Virtual Moore's Law economy (VME) and achieve effective economics beyond the 5 nanometer node or even with an equivalent 3 nanometer node through a new scaling method described as 3D x 3D Microsystem Volume-Scaling for Heterogeneous Integration!

During these past five decades, the IC industry has aggressively pushed for progress and fortunately has also been pulled forward by killer applications, from mainframe computers and telecom switch machines, to PCs and notebooks, to mobile phones and today's smartphones. Now worries have arisen on whether any killer applications will emerge that can sustain semiconductor demand in the future. This talk describes more new killer applications which will continue healthy growth for the semiconductor industry, with values created by heterogeneous integration technology scaling. An emerging era named as Semiconductor-Intelligence Paradigm (SIP), however, will not only be created by scaling devices down, but also by generating more smarter integrations whereby more new technologies will focus on scaling versatile functions up!