2027 VLSI TSA

International VLSI Symposium on Technology, Systems and Applications

April 12–16, 2027 Hsinchu, Taiwan

DAT Call for Papers

Paper Submission Deadline has been extended until 23:59 (GMT+8) on Sunday December 13, 2026

The 2027 International VLSI Symposium on Technology, Systems and Applications (VLSI TSA 2027) will be held on April 12–16, 2027, at the Ambassador Hotel Hsinchu, Taiwan, with an optional excursion scheduled for April 16. Original and unpublished papers on all aspects are solicited, including but not limited to the following scope.

SCOPE

■ **Analog, Mixed-Signal, and RF Design**
- Analog and Mixed-Signal Circuits
- Data Converters
- Power Management Circuits
- Wireless Transmitter and Receiver Circuits
- Wire Line System and IO Design
- Sensor and Interface Circuits

■ **Digital, Memory, and AI Chip Design**
- Asynchronous and Neuromorphic Computing Circuits
- Computing-in-Memory
- Digital AI Chips
- Digital Circuits and ASICs
- Hardware Optimizations for Novel Computation Models
- Hardware Security and Trust Circuits for IoT and AI
- Low Voltage & Ultra Low-Power Circuits and Systems
- Memory Circuits and Systems Including Reliability, Memory Architectures, and Emerging Memories

■ **Application, Software and Hardware, and AI System**
- AI for Systems and Systems for AI
- CPU, DSP, and Multicore Architectures
- Domain-Specific Architectures and Accelerators
- Embedded System and Software
- Hardware-efficient AI Methods
- Multimedia Processing Designs
- SoC (System on Chip) and NoC (Network on Chip)
- Software/Hardware Co-Design and System Compiler
- SiP (System-in-Package) and Heterogeneous Integration

■ **Design Automation and Test Methodology**
- AI for Design Automation & Test
- Behavioral, Logic, and Physical Synthesis
- Design Automation & Test for Analog/Mixed-Signal/RF, 2D/3D IC, Memory, Biochip, AI Chips, and Emerging Systems
- Design for Manufacturability, Testability, and BIST
- Design Verification, Modeling, and Simulation
- Power/Thermal/Timing Optimization and On-Chip Monitoring
- Silicon Debug, Diagnosis, ECO, and Yield/Reliability Enhancement
- Test Generation, Compression, and Test Standards

■ **Emerging Technology**
- Circuit & IP Design Based on New Transistor Technology, e.g., Fork-Fin FET, Sheet FET, GAA FET, and C-FET
- Cryogenic Circuits and Systems
- Flexible and Printable Electronics
- ICs for Harsh Environments and Soft-Error
- Medical/Bio-electronics/Bio-inspired Chip Designs
- Quantum Computing
- Silicon Photonics

GENERAL INSTRUCTIONS

- Prospective authors must electronically submit the self-contained paper with figures and tables via the conference submission page (https://expo.itri.org.tw/2027VLSITSA/DAT/Submission) before November 22, 2026 (23:59 GMT+8).
- The submitted manuscript must be either 2 or 4 pages in length, including references, double-columned, IEEE-style compatible, in PDF format only. Any submissions not adhering to the rules will be rejected immediately without review.
- Before submitting your abstract/paper, please review the information on IEEE Intellectual Property Rights at https://www.ieee.org/publications/rights/index.html
- The review process will be double-blind.
  - Please do NOT reveal any authors' information (names, affiliations, email, grant information, personal acknowledgment, etc.) anywhere in the initial manuscript. You must also ensure that the metadata in the PDF does not include such information.
  - All references, including authors' previous work, should be referred as 3rd-persons' works. E.g., you should use "This paper presents a new method to improve XXX's approach [1]." instead of "This paper presents a new method to improve our previous approach [1]." Do NOT omit or anonymize references for blind review.
  - The initial manuscript violating the double-blind review policy will be rejected.
- Accepted papers MUST be presented in person by one of the authors at the symposium, and the presentation must be conducted in English. All accepted manuscripts in the proceeding will be published in IEEE Xplore.
- Any changes on the title or author list or withdrawal after acceptance must be approved by DAT Program Chairs.
- Author Registration Policy:
  - One FULL Registration covers the publication of up to two accepted papers.
  - Each accepted paper must be covered by a valid full registration in order to be included in the symposium proceedings.
  - If a valid FULL Registration has not been received and processed for an accepted paper, the symposium organizers will contact the authors before the paper is removed from the proceedings.
- No-show papers will not be included in the symposium proceedings and will not be submitted to the IEEE Xplore database.
- Please refer to the detailed information on the conference website for authors: https://expo.itri.org.tw/2027VLSITSA

STUDENT SUBSIDY

Student Travel Financial support for attending VLSI TSA 2027 is available for full-time student presenters living outside of Taiwan.

BEST PAPER AWARD

Three best papers will be selected this year through a rigorous evaluation process conducted by the DAT technical program committee and session chairs.

IMPORTANT DATES (Note: all are based on Taiwan time (GMT+8).)

Regular Paper Submission Deadline	~~November 22~~, 2026 December 13, 2026
Notification of Acceptance	January 27, 2027
Final Paper Submission Deadline	February 28, 2027
Author Registration Deadline	February 28, 2027

DAT Program Chairs:

Hirofumi Shinohara, Kyoto University
Kea-Tiong Tang, National Tsing Hua University
Juin-Ming Lu, Industrial Technology Research Institute