TSIA

2021半導體獎

獎項介紹

「TSIA 半導體獎」是台灣半導體產業協會於 2014 年起，為了獎勵國內積極從事半導體之學術研究、發明或致力投入產業合作並有具體貢獻者而設立。

此獎項之得獎人由本會遴選委員會評選，遴選委員由在半導體領域已有卓越成就之學者、專家及產業領導者擔任。

今年具博士學位之新進研究人員半導體獎由中央大學電機工程學系謝易叡助理教授及陽明交通大學國際半導體產業學院吳添立助理教授獲獎；博士研究生半導體獎得獎者，分別由台大、陽明交通、成大、清大、中山等 5 校 11 位博士班同學獲獎，本會期許得獎人以成為台灣半導體產業優秀貢獻者為目標，再接再厲，為台灣半導體產業之永續發展而戮力前進。

贊助單位：理監事公司

力成科技股份有限公司	力晶科技股份有限公司	力晶積成電子製造股份有限公司
工業技術研究院	日月光半導體製造股份有限公司	世界先進積體電路股份有限公司
立錡科技股份有限公司	台灣積體電路製造股份有限公司	欣銓科技股份有限公司
矽品精密工業股份有限公司	南亞科技股份有限公司	凌陽科技股份有限公司
創意電子股份有限公司	華邦電子股份有限公司	鈺創科技股份有限公司
漢民科技股份有限公司	聯發科技股份有限公司	聯華電子股份有限公司

◎ 以上依公司筆劃順序排列

謝易叡 E Ray Hsieh

國立中央大學 電機工程學系

獲獎摘要

謝易叡助理教授於 2016 年取得國立交通大學電子研究所固態組工程博士學位。他的研究領域專注於半導體元件與電路的設計與整合及相關應用，特別是嵌入式記憶體、前瞻非揮發式記憶體 (RRAM 和 FeRAM) 於 IOT 之應用 (類神經網路運算和資安防護議題)。他在半導體技術頂級旗艦 IEDM 與 VLSI，十年內，以第一作者口頭發表了 20 餘篇電晶體和記憶體相關的學術文章，並共同擁有 30 個美中台三國專利。近年，除學術研究外，謝助理教授更致力於專利商品化，參與台灣積體電路製造公司共同合作開發專案，針對超高密度電阻式記憶體矩陣進行探索。以及謝的研究團隊獨家發展的新型態單次編程記憶體 (OTP) 也接近量產中。此外，謝師獨創的超高密度嵌入式電阻式記憶體三維架構 (3D 1TnR array) 正在進行理論與技術之攻堅，期望為台灣半導體下一個世代的記憶體技術與創新注入新的活力。

得獎經歷

- 2020 年 EDMA (台灣電子材料與元件協會) - 傑出青年獎
- 台灣積體電製造股份有限公司 - 年輕共同開發專案 (TSMC Junior JDP)
- 科技部年輕學者養成計畫 - 愛因斯坦獎勵計畫
- 第 16 屆 (2018 年) 遠東集團徐有庠基金會 - 有庠科技論文獎
- 2018 年科技部 - 博士後研究人員學術著作獎

重要學術著作

1. **E. R. Hsieh**, et al., “Four-bit-per-Memory One-transistor-and-eight-Resistive-random-access-memory,” IEEE-Electron Device Letters (EDL), vol. 42, no. 3, pp. 335-338 (2021).
2. **E. R. Hsieh**, et al., "An Experimental Approach to Characterizing the Channel Local Temperature Induced by Self-Heating Effect in FinFET." IEEE, Journal of the Electron Devices Society (J-EDS), vol. 6, pp. 866-874 (2018).
3. **E. R. Hsieh**, et al., “A 14-nm FinFET Logic CMOS Process Compatible RRAM Flash With Excellent Immunity to Sneak Path,” IEEE, Transactions on Electron Devices, vol. 64, No. 12, pp. 4910-4918 (2017).
4. **E. R. Hsieh**, et al., “The First Embedded 14nm FeFinFET NVM: 2T1CFE Array as Electrical Synapses and Activations for High-performance and Low-power Inference Accelerators,” to be appeared on VLSI Technology, 2021.
5. **E. R. Hsieh**, et al., “A Novel Complementary Architecture of One-timeprogrammable Memory and Its Applications as Physical Unclonable Function (PUF) and One-time Password,” IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2020, pp. 689-692.
6. **E. R. Hsieh**, et al., "High-Density Multiple Bits-per-Cell 1T4R RRAM Array with Gradual SET/RESET and its Effectiveness for Deep Learning," IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2019, pp. 35.6.1- 35.6.4. Tian-Yue Chen, Tsao-Chi Chuang, Ssu-Yen Huang, Hung-Wei Yen, Chi-Feng Pai*, Spin-orbit torque from a magnetic heterostructure of high-entropy alloy (2017, Oct). Physical Review Applied, 8, 044005.
7. **E. R. Hsieh**, et al.,, "The Demonstration of Gate Dielectric-fuse 4kb OTP Memory Feasible for Embedded Applications in High-k Metal-gate CMOS Generations and Beyond," IEEE Symposium on VLSI Circuits, Kyoto, Japan, 2019, pp. C208-C209.
8. **E. R. Hsieh**, et al., "Embedded PUF on 14nm HKMG FinFET Platform: A Novel 2-bit-per-cell OTP-based Memory Feasible for IoT Security Solution in 5G Era," IEEE Symposium on VLSI Technology, Kyoto, Japan, 2019, pp. T118-T119.
9. **E. R. Hsieh**, et al., “First demonstration of flash RRAM on pure CMOS logic 14nm FinFET platform featuring excellent immunity to sneak-path and MLC capability," Symposium on VLSI Technology, Kyoto, 2017, pp. T72-T73.
10. **E. R. Hsieh**, Z. H. Huang, S. S. Chung, J. C. Ke, C. W. Yang, C. T. Tsai, T. R. Yew, "The demonstration of lowcost and logic process fully-compatible OTP memory on advanced HKMG CMOS with a newly found dielectric fuse breakdown," IEEE International Electron Devices Meeting (IEDM), Washington, DC, 2015, pp. 3.4.1-3.4.4.

指導教授 Prof. Steve S. Chung

現職 ・ Emeritus from Department of Electronics Engineering, National Yang Ming Chiao Tung University

學歷 ・ Ph. D. in Electrical Engineering, University of Illinois at Urbana-Champaign

經歷 ・交通大學講座教授（NCTU Chair Professor）
・聯華電子研究講座教授（UMC Research Chair Professor）
・ IEEE Life Fellow

推薦專家 Prof. Simon S. Wong

現職 ・ Department of Electrical Engineering, Stanford University

學歷 ・ Ph.D. in Department of Electrical Engineering, UC Berkeley

經歷 ・ Professor in Dept. of Electrical Engineering, Stanford University
・ IEEE Life Fellow

吳添立 Tian-Li Wu

國立陽明交通大學 國際半導體產業學院

獲獎摘要

吳添立博士就讀於清華大學電子所碩士班期間，開始專注於碳化矽 (SiC) 功率元件的開發。並於比利時魯汶大學 (KU Leuven) 就讀博士班期間，在比利時 imec 內從事於氮化鎵 (GaN) 功率元件開發及可靠度研究。至今已有10年以上寬能隙 (wide bandgap) 氮化鎵 / 碳化矽功率元件研究資歷，並已有超過 80 篇以上國際期刊及研討會論文發表。吳博士團隊在近年來也開始專注於 (1) 鐵電半導體的特性 / 可靠度研究及 (2) 利用人工智慧來協助半導體技術優化，並於 2020 未來科技展展示 AI-Semi 智能優化半導體元件設計、製造及特性平台。此外，吳博士團隊積極參與國際合作，和比利時 imec、美國柏克萊大學 (UC Berkeley)、美國麻省理工學院 (MIT)、美國 IBM、印度德里理工學院 (IIT Delhi)、印度孟買理工學院 (IIT Bombay)、義大利 Padova 大學等有共同合作或論文發表，並曾於國際頂尖會議 2020 VLSI Symposia 上受邀擔任 Mentoring Event 講者，分享個人研究成果、職涯觀點及台灣研究環境。

得獎經歷

- 2020 台灣電機電子工程學院第十屆碩士論文優等指導獎
- 2020 功率半導體材料應用元件國際論壇 - 海報競賽特別獎
- 2020 國立交通大學績優導師
- 2020 英國高等教育學會 Fellow of the Higher Education Academy (FHEA)
- 2019 教育部優秀外國青年來臺蹲點計畫 (TEEP) 績優案例
- 2019 科技部年輕學者養成計畫 (愛因斯坦培植計畫) Young Scholar Fellowship
- 2017 聯發科技青年講座教授

重要學術著作

1. N. Modolo, S.-W. Tang, H.-J. Jiang, C. De Santi, M. Meneghini, and **T.-L. Wu***, "A novel physics-based approach to analyze and model E-mode p-GaN power HEMTs," IEEE Transactions on Electron Devices, vol. 68, no. 4, pp. 1489-1494, April 2021.
2. C.-Y. Chang, C.-S. Wang, C.-Y. Wang, Y.-L. Shen, **T.-L. Wu*** et al., "Demonstration of p-GaN/AlGaN/GaN High Electron Mobility Transistors With an Indium–Tin–Oxide Gate Electrode," IEEE Journal of the Electron Devices Society, vol. 9, pp. 2-5, 2021.
3. **T.-L. Wu*** and S. Kutub, "Machine Learning-Based Statistical Approach to Analyze Process Dependencies on Threshold Voltage in Recessed Gate AlGaN/GaN MIS-HEMTs," IEEE Transactions on Electron Devices, vol. 67, no. 12, pp. 5448-5453, Dec. 2020.
4. Y.-H. Chen, C.-J. Su, T.-H. Yang, C. Hu, and **T.-L. Wu***, "Improved TDDB Reliability and Interface States in 5 nm Hf0.5Zr0.5O2 Ferroelectric Technologies using NH3 Plasma and Microwave Annealing," IEEE Transactions on Electron Devices, vol. 67, no. 4, pp. 1581-1585, Apr. 2020.
5. C. Sharma, N. Modolo, **T.-L. Wu*** et al., "Understanding γ ray Induced Instability in AlGaN/GaN HEMTs using a Physics based Compact Model," IEEE Transactions on Electron Devices, vol. 67, no. 3, pp. 1126-1131, Mar. 2020.
6. **T.-L. Wu***, S.-W. Tang, and H.-J. Jian, "Investigation of Recessed Gate AlGaN/GaN MIS-HEMTs with Double AlGaN Barrier Designs toward an Enhancement-Mode Characteristic," Micromachines, vol. 11, Feb. 2020.
7. Y.-H. Chen, C.-J. Su, C. Hu, and **T.-L. Wu***, "Effects of Annealing on Ferroelectric Hafnium Zirconium Oxide-Based Transistor Technology," IEEE Electron Device Letters, vol. 40, no. 3, pp. 467-470, Mar. 2019.
8. **T.-L. Wu*** et al., "Analysis of the Gate Capacitance-Voltage Characteristics in p-GaN/AlGaN/GaN Heterostructures, " IEEE Electron Device Letters, vol. 38, no. 12, pp.1696-1699, Dec. 2017.
9. **T.-L. Wu*** et al., "Towards Understanding Positive Bias Temperature Instability (PBTI) in Fully Recessed Gate GaN MIS-FETs," IEEE Transactions on Electron Devices, vol. 63, no. 5, pp. 1853-1859, May 2016.
10. **T.-L. Wu*** et al., "Forward Bias Gate Breakdown Mechanism in Enhancement-mode p-GaN gate AlGaN/GaN High-electron-mobility Transistors (HEMTs)," IEEE Electron Device Letters, vol. 36, no. 10, pp. 1001-1003, Oct. 2015.

指導教授 Prof. Guido Groeseneken

現職
- Director of imec PhD research and Academic Relations
- Professor, Electrical Engineering, KU Leuven, Belgium
- Imec Fellow
- IEEE Fellow

學歷
- Ph.D. in Electrical Engineering, KU Leuven, Belgium

經歷
- Manager Device Reliability and Electrical characterization at imec

推薦專家 張翼 教授

現職
- 國立陽明交通大學 / 國際半導體產業學院院長
- 國立陽明交通大學 / 材料工程學系終身講座教授
- 國立陽明交通大學 / 電子與資訊研究中心主任
- 交大 - 台積電聯合研發中心主任
- IEEE Fellow

學歷
- 美國明尼蘇達大學材料科學與工程博士

經歷
- 國立交通大學 / 副校長
- 國立交通大學 / 研發長
- 國立交通大學 / 材料科學與工程學系系主任
- 漢威光電公司 / 總經理

吳俊峯 Chun-Feng Wu

國立台灣大學 資訊工程學系

獲獎摘要

吳俊峯同學自 2016 年起於國立台灣大學資訊工程學研究所攻讀博士班。研究領域包含：記憶體 / 儲存系統、記憶體內運算、作業系統、計算機架構以及嵌入式系統。吳同學於研究領域成果豐碩，曾於 IEEE TC 與 IEEE TCAD 等頂尖國際期刊，及 DAC、CODES+ISSS、EMSOFT、CASES 等 ACM / IEEE 頂尖國際會議以及作業系統領域一等一的會議 USENIX OSDI 中發表論文。

得獎經歷 / 專利

- 科技部 - 博士後千里馬計畫
- 財團法人潘文淵文教基金會 - 潘文淵獎學金
- 財團法人平安菁英基金會 - 菁英獎學金
- 以第四發明人發表美國專利，Patent Number：USP 16,798,166.

重要學術著作

1. **Chun-Feng Wu,** Yuan-Hao Chang, Ming-Chang Yang, and Tei-Wei Kuo, "Joint Management of CPU and NVDIMM for Breaking Down the Great Memory Wall," IEEE Transactions on Computers (TC), vol. 69, no. 5, pp. 722-733, May. 2020.
2. **Chun-Feng Wu,** Yuan-Hao Chang, Ming-Chang Yang, and Tei-Wei Kuo, "When Storage Response Time Catches Up with Overall Context Switch Overhead, What is Next?," accepted and to appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). (Integrated with ACM/IEEE CODES+ISSS'20).
3. **Chun-Feng Wu,** Ming-Chang Yang, Yuan-Hao Chang, and Tei-Wei Kuo, "Hot-Spot Suppression for Resource-Constrained Image Recognition Devices with Non-Volatile Memory," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 37, no. 11, pp. 2567-2577, Nov. 2018. (Integrated with ACM/IEEE EMSOFT 2018)
4. **Chun-Feng Wu,** Ming-Chang Yang, and Yuan-Hao Chang, "Improving Runtime Performance of Deduplication System with Host-Managed SMR Storage Drives," ACM/IEEE Design Automation Conference (DAC), San Francisco, USA, Jun. 24-28, 2018. (Top-Conference)
5. Yao-Wen Kang, **Chun-Feng Wu,** Yuan-Hao Chang, Tei-Wei Kuo and Shu-Yin Ho, "On Minimizing Analog Variation Errors to Resolve the Scalability Issue of ReRAM-based Crossbar Accelerator," accepted and to appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). (Integrated with ACM/IEEE EMSOFT'20).
6. Gaddisa Olani Ganfure, **Chun-Feng Wu,** Yuan-Hao Chang, and Wei-Kuan Shih, "DeepPrefetcher: A Deep Learning Framework for Data Prefetching in Flash Storage Devices," accepted and to appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). (Integrated with ACM/IEEE CASES'20).
7. Ming-Chang Yang, **Chun-Feng Wu,** Shuo-Han Chen, Yi-Ling Lin, Che-Wei Chang, and Yuan-Hao Chang, "On Minimizing Internal Data Migrations of Flash Devices via Lifetime- Retention Harmonization," accepted and to appear in IEEE Transactions on Computers (TC).
8. Yun-Chih Chen, **Chun-Feng Wu,** Yuan-Hao Chang, and Tei-Wei Kuo, "Reptail: Cutting Storage Tail Latency with Inherent Redundancy," ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, USA, Dec. 5-9, 2021. (Top-Conference)
9. Yun-Sheng Chang, Yao Hsiao, Tzu-Chi Lin, Che-Wei Tsao, **Chun-Feng Wu,** Yuan-Hao Chang, Hsiang-Shang Ko, and Yu-Fang Chen, "Determinizing Crash Behavior with a Verified Snapshot-Consistent Flash Translation Layer," USENIX Symposium on Operating Systems Design and Implementation (OSDI), Banff, Alberta, Canada, Nov. 4-6, 2020. (Top- Conference)
10. Shuo-Han Chen, Ming-Chang Yang, Yuan-Hao Chang, and **Chun-Feng Wu,** "Enabling File-Oriented Fast Secure Deletion on Shingled Magnetic Recording Drives," ACM/IEEE Design Automation Conference (DAC), Las Vegas, Nevada, USA, Jun. 2-6, 2019. (Top- Conference)

指導教授　郭大維 教授

現職　・國立台灣大學 / 資訊工程學系特聘教授
・香港城市大學 / 李兆基資訊工程講座教授、校長資深顧問暨工學院院長

學歷　・美國德州大學奧斯汀分校 / 電腦科學博士

經歷　・國立台灣大學 / 代理校長
・國立台灣大學 / 學術副校長
・美國計算機協會會士 ACM Fellow
・國際電機電子工程師學會會士 IEEE Fellow
・美國發明家學院院士 NAI Fellow

共同指導教授　張原豪 研究員

現職　・中央研究院 / 資訊科學研究所

學歷　・國立台灣大學 / 資訊工程博士

經歷　・中央研究院 / 資訊科學研究所副所長
・中央研究院 / 資訊科學研究所研究員

陳天玥 T.-Y. Chen

國立台灣大學 材料科學與工程學系

獲獎摘要

陳天玥同學於 2016 年進入國立台灣大學材料科學與工程學系就讀研究所。研究領域為自旋霍爾效應 (Spin Hall effect)、自旋軌道矩式磁性記憶體 (Spin-Orbit Torque Magnetic Random Access Memory)。曾參與 The Magnetism and Magnetic Materials Conference (MMM), International Conference of Asian Union of Magnetics Societies (IcAUMs) 及 The Magnetic Recording Conference (TMRC) 等國際會議，並於會議中發表相關研究成果。

得獎經歷

- 2020 CTCI Foundation Science and Technology Scholarship
- 2019 USI Education Foundation Scholarship
- 2018 National Taiwan University Outstanding Student Scholarship

重要學術著作

1. **T.-Y. Chen**, C.-T. Wu, H.-W. Yen, and C.-F. Pai, "Tunable spin-orbit torque in Cu-Ta binary alloy heterostructures," Physical Review B 96, 104434 (2017).
2. **T.-Y. Chen**, T.-C. Chuang, S.-Y. Huang, H.-W. Yen, and C.-F. Pai, "Spin-orbit torque from a magnetic heterostructure of high-entropy alloy," Physical Review Applied 8, 044005 (2017).
3. T.-C. Wang, **T.-Y. Chen***, C.-T. Wu, H.-W. Yen, and C.-F. Pai*, "Comparative Study on Spin-Orbit Torque Efficiencies from W/ferromagnetic and W/ferrimagnetic Heterostructures, " Physical Review Materials 2, 014403 (2018).
4. T.-Y. Tsai, **T.-Y. Chen**, C.-T. Wu, H.-I Chan, C.-F. Pai*, "Spin-orbit torque magnetometry by wide-field magneto-optical Kerr effect" Scientific Reports 8, 5613 (2018).
5. **T.-Y. Chen**, H.-I. Chan, W.-B. Liao, and C.-F. Pai*, "Current-induced spin-orbit torque and field-free switching from Mo-based magnetic heterostructures," Physical Review Applied 10, 044038 (2018).
6. **T.-Y. Chen**, Y. Ou, T.-Y Tsai, R. A. Buhrman, and C.-F. Pai*, "Spin-orbit torques acting upon a perpendicularly-magnetized Py layer," APL Materials 6, 121101 (2018).
7. W.-B. Liao, **T.-Y. Chen**, Y. Ferrante, S. S. P. Parkin, and C.-F. Pai*, "Current-induced magnetization switching by the high spin Hall conductivity α-W," Physica Status Solidi (RRL) - Rapid Research Letters 13, 1900408 (2019).
8. **T.-Y. Chen**, C.-W. Peng, T.-Y. Tsai, W.-B. Liao, C.-T. Wu, H.-W. Yen, and C.-F. Pai*, "Efficient Spin-Orbit Torque Switching with Nonepitaxial Chalcogenide Heterostructures," ACS Appl. Mater. Interfaces 12, 7788 (2020).
9. Y.-T. Liu, **T.-Y. Chen***, T.-H. Lo, T.-Y. Tsai, S.-Y. Yang, Y.-J. Chang, J.-H. Wei, and C.-F. Pai*, "Determination of Spin-Orbit Torque Efficiencies in Heterostructures with In-plane Magnetic Anisotropy," Physical Review Applied 13, 044032 (2020).
10. W.-B. Liao, **T.-Y. Chen**, Y.-C. Hsiao, and C.-F. Pai*, "Pulse-width and Temperature Dependence of Memristive Spin-Orbit Torque Switching," Applied Physics Letters 117, 182402 (2020).

指導教授　白奇峰 副教授

現職　・國立台灣大學

學歷　・ Ph.D. in Applied Physics, Cornell University

經歷　・ 2014 - 2016　Post-doctoral Research Associate, DMSE, MIT

・ 2016 - present　Consulting Research Fellow, MRAM Team, ITRI

・ 2019 - present　Vice Chair, IEEE Magnetic Society, Taiwan Chapter

鄒亞叡 Ya-Jui Tsou

國立台灣大學 電子工程學研究所

獲獎摘要

鄒亞叡同學於國立台灣大學電子工程學研究所攻讀博士班，研究領域為自旋轉移力矩與自旋軌道力矩磁阻式記憶體 (STT-MRAM & SOT-MRAM)，開發垂直式磁穿隧接面 (MTJ) 薄膜沉積與優化、離子束蝕刻以製備磁性元件、LLG 物理等效模型分析寫入容忍度、磁阻式記憶體陣列的自發熱效應模擬。相關研究成果發表於 IEEE 頂尖國際會議 Symposium on VLSI Technology、IEDM MRAM Poster、JXCDC 國際期刊，有 8 項美國專利申請中。成果豐碩，難能可貴。

得獎經歷 / 專利

- 2020 台大 1975 級電機系系友科技研究創新獎
- 2017~2020 台積電 - 台大聯合研發中心獎助學金
- 以第一發明人申請 3 篇美國專利，以共同發明人申請 5 篇美國專利

重要學術著作

1. **Ya-Jui Tsou**, Kai-Shin Li, Jia-Min Shieh, Wei-Jen Chen, Hsiu-Chih Chen, Yi-Ju Chen, Cho-Lun Hsu, Yao-Min Huang, Fu-Kuo Hsueh, Wen-Hsien Huang, Wen-Kuan Yeh, Huan-Chi Shih, Pang-Chun Liu, C. W. Liu, Yu-Shen Yen, Chih-Huang Lai, Jeng-Hua Wei, Denny D. Tang, and Jack Yuan-Chen Sun, "First Demonstration of Interface-Enhanced SAF Enabling 400°C-Robust 42 nm p-SOT-MTJ Cells with STT-Assisted Field-Free Switching and Composite Channels," Symposia on VLSI Technology and Circuits (VLSI), Jun. 2021.
2. **Ya-Jui Tsou**, Jih-Chao Chiu, Huan-Chi Shih, and C. W. Liu, "Write Margin Analysis of Spin-Orbit Torque Switching Using Field-Assisted Method," IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JXCDC), vol. 5, no. 2, pp. 173-181, Dec. 2019.
3. **Ya-Jui Tsou**, Chia-Che Chung, Jih-Chao Chiu, Huan-Chi Shih, and C. W. Liu, "Thermal and Reliability Modeling of FinFET-Driven STT-pMTJ Array Considering Mutual Coupling, 3D Heat Flow, and BEOL Effects," IEDM MRAM Poster, Dec. 2019.
4. **Ya-Jui Tsou**, Zong-You Luo, Chia-Che Chung, and C. W. Liu, "Thermal Modeling of FinFET-Driven Spin-Orbit Torque MRAM Considering Thermal Coupling and BEOL Effects," IEDM MRAM Poster, Dec. 2018.
5. Jih-Chao Chiu, **Ya-Jui Tsou**, Huan-Chi Shih, and C. W. Liu, "Write Error Rate Prediction of STT-pMTJ Considering Process Variations and Thermal Fluctuations," IEDM MRAM Poster, Dec. 2019.
6. Zong-You Luo, **Ya-Jui Tsou**, and C. W. Liu, "Field-Free Spin-Orbit Torque Switching of pMTJ Utilizing Voltage-Controlled Magnetic Anisotropy and STT," IEDM MRAM Poster, Dec. 2018.
7. Zong-You Luo, **Ya-Jui Tsou**, Yi-Cheng Dong, Ching Lu, and C. W. Liu, "Field-free Spin-orbit Torque Switching of Perpendicular Magnetic Tunnel Junction Utilizing Voltage-Controlled Magnetic Anisotropy Pulse Width Optimization," Non-Volatile Memory Technology Symposium (NVMTS), Oct. 2018.
8. Yu-Shiang Huang, **Ya-Jui Tsou**, Chih-Hsiung Huang, Chih-Hao Huang, Huang-Siang Lan, C. W. Liu, Yi-Chiau Huang, Hua Chung, Chorng-Ping Chang, Schubert S. Chu, and Satheesh Kuppurao, "High-Mobility CVD-Grown Ge/Strained $Ge_{0.9}Sn_{0.1}$/Ge Quantum-Well pMOSFETs on Si by Optimizing Ge Cap Thickness," IEEE Transactions on Electron Devices, vol. 64, no. 6, pp. 2498-2504, Jun. 2017.
9. Yu-Shiang Huang, Fang-Liang Lu, **Ya-Jui Tsou**, Hung-Yu Ye, Shih-Ya Lin, Wen-Hung Huang, and C. W. Liu, "Vertically Stacked Strained 3-GeSn-Nanosheet pGAAFETs on Si Using GeSn/Ge CVD Epitaxial Growth and the Optimum Selective Channel Release Process," IEEE Electron Device Letters, vol. 39, no. 9, pp. 1274-1277, Sep. 2018.
10. Yu-Shiang Huang, Fang-Liang Lu, **Ya-Jui Tsou**, Chung-En Tsai, Chung-Yi Lin, Chih-Hao Huang, and C. W. Liu, "First Vertically Stacked GeSn Nanowire pGAAFETs with Ion=1850 μA/μm (V_{OV}=V_{DS}=-1V) on Si by GeSn/Ge CVD Epitaxial Growth and Optimum Selective Etching," International Electron Devices Meeting (IEDM), pp. 832-835, Dec. 2017.

指導教授　劉致為 教授

現職
- Distinguished Professor / Chair Professor of Electrical Engineering, National Taiwan University

學歷
- Ph.D. 1994 in Electrical Engineering, Princeton University
- M.S. 1987 and B.S. 1985 in Electrical Engineering, National Taiwan University

經歷
- IEEE Fellow (2018~)
- Deputy General Director (副主任 , 2008~2013) / Senior full researcher (資深研究員 , 2011~), National Nano Device Laboratories
- Research Director / Senior full researcher (資深研究員), ERSO / ITRI (2002 ~ 2005)

蔡仲恩 Chung-En Tsai

國立台灣大學 電子工程學研究所

獲獎摘要

蔡仲恩同學於國立台灣大學電子工程學研究所攻讀博士班，研究領域為化學氣相沉積 (CVD) 系統之四族磊晶成長，並探討高硼摻雜濃度對鍺錫接觸電阻之影響，以及將原子層沉積法 (ALD) 成長之功函數金屬整合於 3D 電晶體以調變元件之臨界電壓。相關研究成果發表於 IEEE 頂尖國際會議 Symposium on VLSI Technology 與 IEDM 和一流之 IEEE TED 國際期刊。成果豐碩，難能可貴。

得獎經歷 / 專利

- 以第一發明人發表美國專利，Patent number：USP 10,777,663
- 以第五發明人發表美國專利，Patent number：USP 10,957,784 and 10,332,985
- 以第七發明人發表美國專利，Patent number：USP 10,340,383
- 2016 - 2020 台積電 - 臺大聯合研發中心獎助學金

重要學術著作

1. **Chung-En Tsai**, Yu-Rui Chen, Chien-Te Tu, Yi-Chun Liu, Jyun-Yan Chen, and C. W. Liu, "First Demonstration of Multi-V_T Stacked $Ge_{0.87}Sn_{0.13}$ Nanosheets by Dipole-Controlled ALD WNxCy Work Function Metal with Low Resistivity and Thermal Budget ≤ 400 °C," Symposia on VLSI Technology and Circuits (VLSI), 2021.
2. Yi-Chun Liu, Chien-Te Tu, **Chung-En Tsai**, Yu-Rui Chen, Jyun-Yan Chen, Sun-Rong Jan, Bo-Wei Huang, Shee-Jier Chueh, Chia-Jung Tsen, and C. W. Liu, "First Highly Stacked $Ge_{0.95}Si_{0.05}$ nGAAFETs with Record I_{ON} = 110 μA (4100 μA/μm) at V_{OV}=V_{DS}=0.5V and High $G_{m,max}$ = 340 μS (13000 μS/μm) at V_{DS}=0.5V by Wet Etching," Symposia on VLSI Technology and Circuits (VLSI), 2021.
3. Yu-Shiang Huang, **Chung-En Tsai**, Chien-Te Tu, Jyun-Yan Chen, Hung-Yu Ye, Fang-Liang Lu, and C. W. Liu, "First Demonstration of Uniform 4-Stacked $Ge_{0.9}Sn_{0.1}$ Nanosheets with Record I_{ON}=73 μA at V_{OV}=V_{DS}= -0.5V and Low Noise Using Double $Ge_{0.95}Sn_{0.05}$ Caps, Dry Etch, Low Channel Doping, and High S/D Doping," pp. 23-26, International Electron Devices Meeting (IEDM), 2020.
4. **Chung-En Tsai**, Fang-Liang Lu, Yi-Chun Liu, Hung-Yu Ye, and C. W. Liu, "Low Contact Resistivity to Ge Using In-situ B and Sn Incorporation by Chemical Vapor Deposition," IEEE Transactions on Electron Devices, Vol. 67, No. 11, pp. 5053-5058, Nov. 2020.
5. Yu-Shiang Huang, Fang-Liang Lu, Chien-Te Tu, Jyun-Yan Chen, **Chung-En Tsai**, Hung-Yu Ye, Yi-Chun Liu and C. W. Liu, "First Demonstration of 4-Stacked $Ge_{0.915}Sn_{0.085}$ Wide Nanosheets by Highly Selective Isotropic Dry Etching with High S/D Doping and Undoped Channels," Symposia on VLSI Technology and Circuits (VLSI), 2020.
6. Fang-Liang Lu, Yi-Chun Liu, **Chung-En Tsai**, Hung-Yu Ye, and C. W. Liu, "Record Low Contact Resistivity to Ge:B ($8.1x10^{-10}$Ω-cm^2) and GeSn:B ($4.1x10^{-10}$Ω-cm^2) with Optimized [B] and [Sn] by In-situ CVD Doping," Symposia on VLSI Technology and Circuits (VLSI), 2020.
7. **Chung-En Tsai**, Chih-Hsiung Huang, Yu-Rui Chen, Chien-Te Tu, Yu-Shiang Huang, and C. W. Liu, "600 meV Effective Work Function Tuning by Sputtered WNx Films," 2020 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), Hsinchu, April 20-23, 2020.
8. Yu-Shiang Huang, **Chung-En Tsai**, Chien-Te Tu, Hung-Yu Ye, Yi-Chun Liu, Fang-Liang Lu, and C. W. Liu, "First Stacked $Ge_{0.88}Sn_{0.12}$ pGAAFETs with Cap, L_G=40nm, Compressive Strain of 3.3%, and High S/D Doping by CVD Epitaxy Featuring Record I_{ON} of 58 μA at V_{OV}=V_{DS}= -0.5V, Record $G_{m,max}$ of 172 μS at V_{DS}= -0.5V, and Low Noise," pp. 689-692, International Electron Devices Meeting (IEDM), 2019.
9. Fang-Liang Lu, **Chung-En Tsai**, Chih-Hsiung Huang, Hung-Yu Ye, Shih-Ya Lin, C. W. Liu, "Record Low Contact Resistivity ($4.4x10^{-10}$Ω-cm^2) to Ge Using In-situ B and Sn Incorporation by CVD With Low Thermal Budget (≤400 ℃) and Without Ga," pp.178-179, Symposia on VLSI Technology and Circuits (VLSI), 2019.
10. **Chung-En Tsai**, Fang-Liang Lu, Pin-Shiang Chen, and C. W. Liu, "Boron-doping induced Sn loss in GeSn alloys grown by chemical vapor deposition," Thin Solid Films, Vol. 660, pp. 263-266, 2018.

指導教授　劉致為 教授

現職 ・ Distinguished / Chair Professor, National Taiwan University

學歷 ・ Ph.D. 1994 Electrical Engineering, Princeton University
・ M.S. 1987 and B.S. 1985, National Taiwan University

經歷 ・ IEEE Fellow (2018~)
・ Deputy General Director (副主任 , 2008~2013) / Senior full researcher (資深研究員 , 2011~), National Nano Device Labs
・ Research Director / Senior full researcher (資深研究員), ERSO / ITRI (2002 ~ 2005)

呂紹永 Shao-Yung Lu

國立陽明交通大學 電機工程研究所

獲獎摘要

呂紹永同學於國立陽明交通大學電機工程研究所攻讀博士班。研究領域包含電化學感測前端電路(Electrochemical sensing front end circuit) 開發與高精準低功耗振盪器研究。至今累積發表國際期刊與國際研討會議論文17篇。於國際權威固態電路會議 ISSCC 發表應用於傷口照護之電化學全整合感測晶片，並獲得當年度 ISSCC 遠東論文獎 (Silkroad Award)。此外，低功耗高精準振盪器發表於頂尖固態電路期刊 JSSC，研究成果豐碩。

得獎經歷

- 2021 ISSCC Silkroad Award 遠東論文獎
- 2017、2020 光寶創新獎 Merit Award
- 2018、2020 旺宏金矽獎優勝
- 2020 科技部未來科技獎
- 2016、2017 TSRI 優良 / 特優晶片設計獎
- 2019 聯詠科技博士班獎學金
- 2018 思源博士班獎學金

重要學術著作

1. **Shao-Yung Lu**, Siang-Sin Shan, Shih-Che Kuo, Cheng-Ze Shao, Yung-Hua Yeh, I-Te Lin, Shu-Ping Lin, Yu-Te Liao , A Wireless Multimodality System-on-a-Chip with Time-Based Resolution Scaling Technique for Chronic Wound Monitoring," IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2021, pp. 282-284
2. **Shao-Yung Lu**, Siang-Sin Shan, Ting-Heng Lu, Yung-Hua Yeh, Shi-Zhe Guo, Yi-Chia Chen, Yu-Te Liao, "A Review of CMOS Electrochemical Readout Interface Designs for Biomedical Assays," IEEE Sensors Journal, 2021(Accepted)
3. **Shao-Yung Lu** and Yu-Te Liao, "A 19 μW, 50 kS/s, 0.008-400 V/s Cyclic Voltammetry Readout Interface with a Current Feedback Loop and On-Chip Pattern Generation" IEEE Transactions on Biomedical Circuits and Systems, 2021 (Accepted)
4. **Shao-Yung Lu**, Siang-Sin Shan, Tiger Chang, Yu-Te Liao, "A Wide-Range Capacitance-to-Frequency Readout Circuit using Pulse-Width Detection and Delay-Line-Based Feedback Control Loop," IEEE International Symposium on Circuits and Systems (ISCAS), Sevilla, Sep. 2020, pp. 1-5
5. Siang-Sin Shan, **Shao-Yung Lu**, Yuan-Po Yang, Shu-Ping Lin, Patrick Carey, Minghan Xian, Fan Ren, Stephen Pearton, Chin-Wei Chang, Jenshan Lin, Yu-Te Liao, "A Two-Electrode, Double-Pulsed Sensor Readout Circuit for Cardiac Troponin I Measurement," IEEE Transactions on Biomedical Circuits and Systems, vol. 14, no. 6, pp. 1362-1370, Dec. 2020
6. **Shao-Yung Lu** and Yu-Te Liao, "A Low-Power, Differential Relaxation Oscillator With the Self-Threshold-Tracking and Swing-Boosting Techniques in 0.18-um CMOS," IEEE Journal of Solid-State Circuits, vol. 54, no. 2, pp. 392-402, Feb. 2019
7. **Shao-Yung Lu**, Siang-Sin Shan, Jiancheng Yang, Chin-Wei Chang, Fan Ren, Jenshan Lin, Stephen Pearton, Yu-Te Liao,"A Reconfigurable, Pulse-shaping Potentiometric Readout System for Bio-Sensing Transistors," 41st Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), Berlin, Germany, July 2019, pp. 5761-5764
8. Yi-Chia Chen, **Shao-Yung Lu** and Yu-Te Liao, "A Microwatt Dual-Mode Electrochemical Sensing Current Readout With Current-Reducer Ramp Waveform Generation," IEEE Transactions on Biomedical Circuits and Systems, vol. 13, no. 6, pp. 1163-1174, Dec. 2019
9. **Shao-Yung Lu** and Yu-Te Liao, "A 46 μW, 8.2MHz self-threshold-tracking differential relaxation oscillator with 7.66psrms period jitter and 1.56ppm allan deviation floor," IEEE Custom Integrated Circuits Conference (CICC), San Diego, CA, Apr. 2018, pp. 1-4
10. Fu-To Lin, **Shao-Yung Lu**, Yu-Te Liao, "A 2.2 uW, -12 dBm RF-Powered Wireless Current Sensing Readout Interface IC With Injection-Locking Clock Generation," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 7, pp. 950-959, July 2016

指導教授　廖育德 教授

現職　・國立陽明交通大學 / 電機工程學系
學歷　・美國華盛頓大學 / 電機工程學系博士
經歷　・美國佛羅里達大學訪問學者 (2018)
・ IEEE Sensors Journal Associate Editor (2017~)
・國立陽明交通大學 / 電機工程學系教授 (2020~)

鍾昀晏 Yun-Yan Chung

國立陽明交通大學 電子工程研究所

獲獎摘要

鍾昀晏同學自 2016 年起大學逕讀國立陽明交通大學電子工程研究所博士班。研究領域為二維材料電晶體開發 (Two-dimensional material transistor development)，探討接觸電阻 (contact resistance) 與二維材料元件應用 (Two-dimensional material device application)，並且提出相應的解決方案。成果分別發表於 IEEE EDL (2 篇第一作者)、IEEE TED (1篇第一作者)、於 2019 年 IEEE VLSI (第一學生作者) 與 2020 年 IEEE IEDM (第一作者)，2 項專利申請中。在學期間成果豐碩，難能可貴。

得獎經歷 / 專利

- 2019 交大台積電聯合研發中心獎助學金
- 2020 交大台積電聯合研發中心獎助學金
- 專利 “A Novel Contralateral-Gated Transistor for Logic Circuit, Embedded Memory & Artificial Intelligence in Back-End-of-Line Application” 第一專利發明人
- 專利 “Two-dimensional material transistor with triple-gate design to realize NAND and NOR logic computing” 第一專利發明人

重要學術著作

1. **Yun-Yan Chung**, Chao-Ching Cheng, Bo-Kai Kang, Wei-Chen Chueh, Shih-Yun Wang, Chen-Han Chou, Terry Y.T. Hung, Shin-Yuan Wang, Wen-Hao Chang, Lain-Jong Li and Chao-Hsin Chien, “Switchable NAND and NOR Logic Computing in Single Triple-Gate Monolayer MoS_2 n-FET.” IEEE International Electron Devices Meeting (IEDM), 12-18 Dec. 2020.
2. Terry Y.T. Hung, Shih-Yun Wang, Chih-Piao Chuu, **Yun-Yan Chung**, Ang-Sheng Chou, Feng-Shew Huang, Tac Chen, Ming-Yang Li, Chao-Ching Cheng, Jin Cai, Chao-Hsin Chien, Wen-Hao Chang, H.-S. Philip Wong and Lain-Jong Li, “Pinning-Free Edge Contact Monolayer MoS_2 FET.” IEEE International Electron Devices Meeting (IEDM), 12-18 Dec. 2020.
3. Chao-Ching Cheng, **Yun-Yan Chung**, Ming-Yang Li, Chao-Ting Lin, Chi-Feng Li, Jyun-Hong Chen, Tung-Yen Lai, Kai-Shin Li, Jia-Min Shieh, Sheng-Kai Su, Hung-Li Chiang, Tzu-Chiang Chen, Lain-Jong Li, H.-S. Philip Wong, and Chao-Hsin Chien. “First demonstration of 40-nm channel length top-gate WS_2 pFET using channel area-selective CVD growth directly on SiO_X/Si substrate” IEEE Symposium on VLSI Technology, 9-14 Jun. 2019.
4. **Yun-Yan Chung**, Chao-Ching Cheng, Yu-Che Chou, Wei-Chen Chueh, Wan-Hsuan Chung, Zhi-Hao Yu, Terry Yi-Tse Hung, Lin-Yun Huang, Shin-Yuan Wang, Li-Cheng Teng, Wen-Hao Chang, Lain-Jong Li, and Chao-Hsin Chien. “High Accuracy Deep Neural Networks Using Contralateral-Gated Analog Synapse Composed of ultra-thin MoS_2 nFET and Nonvolatile Charge-Trap Memory” IEEE Electron Device Letter, Vol. 41, No. 11, pp. 1649-1652, Nov. 2020.
5. **Yun-Yan Chung**, Kuan-Cheng Lu, Chao-Ching Cheng, Ming-Yang Li, Chao-Ting Lin, Chi-Feng Li, Jyun-Hong Chen, Tung-Yen Lai, Kai-Shin Li, Jia-Min Shieh, Sheng-Kai Su, Hung-Li Chiang, Tzu-Chiang Chen, Lain-Jong Li, H.-S. Philip Wong, Wen-Bin Jian and Chao-Hsin Chien. “Demonstration of 40-nm Channel Length Top-gate p-MOSFET of WS_2 Channel Directly Grown on SiO_X/Si Substrates Using Area-Selective CVD Technology” IEEE Transactions on Electron Device, Vol. 66, No. 12, pp. 5381-5386, Dec. 2019.
6. **Yun-Yan Chung**, Chi-Feng Li, Chao-Ting Lin, Yen-Teng Ho and Chao-Hsin Chien. “Experimentally Determining the Top and Edge Contact Resistivities of Two-Step Sulfurization Nb-Doped MoS_2 Films Using the Transmission Line Measurement” IEEE Electron Device Letter, Vol. 40, No. 10, pp. 1662-1665, Oct. 2019.
7. **Yun-Yan Chung**, Ming-Li Tsai, Yen-Teng Ho, Yuan-Chieh Tseng and Chao-Hsin Chien. “Study of the Band Alignment between Atomic-Layer-Deposited High-κ Dielectrics and MoS_2 Film” ECS Journal of Solid State Science and Technology, Vol. 7, No. 4, 10 Apr. 2018.
8. Yi-He Tsai, Chen-Han Chou, **Yun-Yan Chung**, Wen-Kuan Yeh, Fu-Hsiang Ko and Chao-Hsin Chien. “Demonstration of HfO_2-Based Gate Dielectric with Low Interface State Density and Sub-nm EOT on Ge by Incorporating Ti into Interfacial Layer” IEEE Electron Device Letter, Vol. 40, No. 2, pp. 174-176, Feb. 2019.

指導教授 簡昭欣 教授

現職 ・國立陽明交通大學 / 電子工程研究所教授
學歷 ・國立交通大學 / 電子工程博士
經歷 ・國立交通大學 / 電子系所教授（2010/8）
・國立交通大學 / 電子系所副教授（2007/8）
・國立交通大學 / 電子系所助理教授（2005/8）
・國家奈米元件實驗室 / 副研究員（1999/9）

共同指導教授 鄭兆欽 技術經理

現職 ・台灣積體電路製造股份有限公司 / 合作研究處
學歷 ・國立交通大學 / 電子工程博士
經歷 ・台積電 / 合作研究處技術經理（2020/7）
・台積電 / 先進元件研究處技術副理 （2013/7）

王建評 Chien-Ping Wang

國立清華大學 電子工程研究所

獲獎摘要

王建評同學自 2019 年起於國立清華大學電子工程研究所攻讀博士班。目前主要研究領域為包含 CMOS 離子感測器 (Ion Sensor) 與應用於先進製程之電子束 (Electron Beam, e-beam) 感測器與新型高密度與高解析度之光學感測器，包含極紫外光 (Extreme Ultraviolet, EUV) 與深紫外光 (Deep Ultraviolet, DUV) 之感測監控與參數萃取。研究成果曾於 IEDM 與 Sym. on VLSI 等 IEEE 頂尖國際會議發表。

得獎經歷

- 2020 台積電研究助理獎學金
- 2019 鑫淼基金會重點科技博士生獎學金計畫
- 2019 科技部 - 培育優秀博士生獎學金
- 2019 台積電研究助理獎學金
- 2018 台積電研究助理獎學金
- 2017 台積電研究助理獎學金

重要學術著作

1. **Chien-Ping Wang**, Burn Jeng Lin, Jiaw-Ren Shih, Yue-Der Chih, Jonathan Chang, Chrong Jung Lin and Ya-Chin King*, "On-Wafer Electronic Layer Detectors Array (ELDA) for e-beam Imaging in Advanced Lithographic Systems," in 2021 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), Hsinchu, Apr. 2021.
2. **Chien-Ping Wang**, Ying-Chun Shen, Kun-Lin Liou, Yu-Lun Chueh, Yue-Der Chih, Jonathan Chang, Jiaw-Ren Shih, Chrong Jung Lin and Ya-Chin King*, "Hair-Like Nanostructure Based Ion Detector by 16nm FinFET Technology," in 2020 IEEE Symposia on VLSI Technology and Circuits (Sym. on VLSI), Honolulu, HI, June 2020.
3. **Chien-Ping Wang**, Yi-Pei Tsai, Burn Jeng Lin, Zheng-Yong Liang, Po-Wen Chiu, Jiaw-Ren Shih, Chrong Jung Lin and Ya-Chin King*, "On-Wafer FinFET-Based EUV/eBeam Detector Arrays for Advanced Lithography Processes," in IEEE Transactions on Electron Devices (TED), vol. 67, no. 6, pp. 2406-2413, April 2020.
4. **Chien-Ping Wang**, Ying-Chun Shen, Peng-Chun Liou, Yu-Lun Chueh, Yue-Der Chih, Jonathan Chang, Chrong-Jung Lin and Ya-Chin King*, "Dynamic pH Sensor with Embedded Calibration Scheme by Advanced CMOS FinFET Technology," in Sensors, vol. 19, no. 7, pp. 1585, April 2019.
5. Zih-Hong Chen, Po-Hsiang Huang, **Chien-Ping Wang**, Yu-Der Chih, Chrong-Jung Lin and Ya-Chin King*, "Embedded Near-Infrared Sensor with Tunable Sensitivity for Nanoscale CMOS Technologies," in IEEE Sensors Journal, vol. 19, no. 3, pp. 933-939, Feb.1, 2019.
6. Peng-Chun Liou, Tsung-Han Lee, **Chien-Ping Wang**, Yu-Lun Chueh, Yue-Der Chih, Jonathan Chang, Chrong Jung Lin, Ya-Chin King*, "High Resolution Ion Detector (HRID) by 16nm FinFET CMOS Technology," in 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, Dec. 2018.
7. Zih-Hong Chen, **Chien-Ping Wang**, Po-Hsiang Huang, Chrong Jung Lin and Ya-Chin King*, "Embedded Tunable Near Infrared Sensor with Programmable Potential Barrier on Nano-meter CMOS Platforms," in 2018 IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM), Kobe, Mar. 2018, pp. 274-276.

指導教授 金雅琴 教授

現職 ・國立清華大學 / 電子工程研究所
・國立清華大學 / 先進快閃記憶體中心主任

學歷 ・Ph.D. 1999 and MS. 1994 Electrical Engineering, University of California, Berkeley,BS. 1992 Electrical Engineering, National Taiwan University

經歷 ・國立清華大學 / 電子工程研究所教授 (1999~)

共同指導教授 林崇榮 教授

現職 ・國立清華大學 / 電子工程研究所
・世界先進積體電路股份有限公司 (VIS) (借調)

學歷 ・Ph.D. 1996, MS. 1992 and BS. 1990, Electrical Engineering, National Tsing Hua University

經歷 ・國立清華大學 / 電子工程研究所 教授 (2005~)
・世界先進積體電路股份有限公司 (VIS) (借調) (2015~)
・台灣積體電路製造公司 (TSMC) Program Manager, R&D (1996~2005)

薛承昕 Cheng-Xin Xue

國立清華大學 電機工程學系

獲獎摘要

薛承昕同學自 2017 年起於國立清華大學電機工程學系-系統組攻讀博士班。主要研究領域為應用於人工智能晶片之記憶體內運算 (Computing-in-memory,CIM) 電路設計。其中包含揮發性記憶體內運算架構 SRAM-CIM 及非揮發性記憶體內運算架構 ReRAM-CIM。其研究成果於國際頂級期刊 Nature Electronics, JSSC 及 ISSCC、IEDM、ASSCC 等 IEEE 頂尖國際會議發表。

得獎經歷

- 2021 台積電獎學金
- 2020 旺宏金矽獎 - 優勝
- 2020 台積電獎學金
- 2019 台積電獎學金
- 2019 旺宏金矽獎 - 銅獎
- 2018 旺宏金矽獎 - 銅獎

重要學術著作

1. **Cheng-Xin Xue**, et.al, "A CMOS-integrated compute-in-memory macro based on resistive random-access memory for AI edge devices," Nature Electronics, vol. 4, pp.81-90, Jan. 2021 (Research Article)
2. **Cheng-Xin Xue**, et.al, "A 22nm 4Mb 8b-Precision ReRAM Computing-in-Memory Macro with 11.91 to 195.7TOPS/W for Tiny AI Edge Devices." IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers, Feb. 2021.
3. **Cheng-Xin Xue**, et.al, "Embedded 1-Mb ReRAM-Based Computing-in-Memory Macro With Multibit Input and Weight for CNN-Based AI Edge Processors." IEEE Journal of Solid-State Circuits (JSSC), vol.55, No. 1, pp.203-215, Jan. 2020.
4. **Cheng-Xin Xue**, et.al, "A 22nm 2Mb ReRAM Compute-in-Memory Macro with 121-28TOPS/W for Multibit MAC Computing for Tiny AI Edge Devices." IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers, pp.244-245, Feb. 2020.
5. **Cheng-Xin Xue**, et.al, "A 1Mb Multibit ReRAM Computing-In-Memory Macro with 14.6ns Parallel MAC Computing Time for CNN Based AI Edge Processors." IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers, pp.388-389, Feb. 2019.
6. Fu-Kuo Hsueh …**Cheng-Xin Xue**, et.al, "Monolithic 3D SRAM-CIM Macro Fabricated with BEOL Gate-All-Around MOSFETs." IEEE International Electron Devices Meeting (IEDM), pp.54-57, Nov. 2019.
7. **Cheng-Xin Xue**, et.al, "A 28-nm 320-Kb TCAM Macro Using Split-Controlled Single-Load 14T Cell and Triple-Margin Voltage Sense Amplifier." IEEE Journal of Solid-State Circuits (JSSC), Vol. 54, No. 10, pp.2743-2753, Oct. 2019.
8. Wei-Hao Chen, … **Cheng-Xin Xue**, et.al, "CMOS-integrated memristive non-volatile computing-in-memory for AI edge processors" Nature Electronics, Vol. 2, No. 9, pp.420-428, Sep. 2019.
9. **Cheng-Xin Xue**, et.al, " A 28mn 320Kb TCAM Macro with Sub-0.8ns Search Time and 3.5+x Improvement in Delay-Area-Energy Product using Split-Controlled Single-Load 14T Cell." IEEE Asian Solid-State Circuits Conference (A-SSCC), pp.127-128, Nov. 2018.
10. Wei-Hao Chen,…**Cheng-Xin Xue**, et.al," A 65nm 1Mb nonvolatile computing-in-memory ReRAM macro with sub-16ns multiply-and-accumulate for binary DNN AI edge processors." IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers, pp.494-496, Feb. 2018.

指導教授　張孟凡 教授

現職　・國立清華大學 / 電機工程學系特聘教授
・台灣積體電路製造公司（TSMC）Director of Corporate Research

學歷　・國立交通大學 / 電子工程博士

經歷　・ IEEE Fellow（2019 年）
・台灣積體電路製造公司（TSMC）Director of Corporate Research（2020~）
・ IEEE Taipei Section Chair (2019/1-2021/1)
・科技部 Program Director, Micro-Electronics Program (2018/1-2020/12)
・國立清華大學 / 電機工程學系特聘教授（2019/8 ~）
・國立清華大學 / 電機工程學系教授（2014/8）
・國立清華大學 / 電機工程學系副教授（2006/8）

黃一平 Ying-Ping Huang

國立成功大學 微電子研究所

獲獎摘要

黃一平同學自 2015 年起於國立成功大學微電子研究所攻讀博士班。主要研究領域為氮化鎵功率元件及高頻元件，其中所研製出的新型三閘極奈米線氮化鎵元件在功率應用領域上，性能達到目前已發表中最頂尖的水準。研究成果曾於國際一流期刊 IEEE Electron Device Letter、IEEE Transactions on Electron Devices 及國際一流研討會 Device Research Conference 上發表，並有論文有幸被 IEEE Electron Device Letter 期刊選為期刊封面及重點論文。

重要學術著作

1. **Ying-Ping Huang**, Wei-Chou Hsu, Han-Yin Liu, and Ching-Sung Lee, "Enhancement-Mode Tri-Gate Nanowire InAlN/GaN MOSHEMT for Power Applications," IEEE Electron Device Lett., vol. 40, no. 6, pp. 929-932, Jun. 2019.
2. **Ying-Ping Huang**, Chih-Chieh Huang, Ching-Sung Lee, and Wei-Chou Hsu, "Enhancement-Mode InAlN/GaN Power MOSHEMT on Silicon With Schottky Tri-Drain Extension," IEEE Trans. Electron Devices, vol. 67, no. 12, pp. 5434-5440, Jul. 2020.
3. **Ying-Ping Huang**, Ching-Sung Lee, and Wei-Chou Hsu, "Normally-Off InAlN/GaN Fin-MOSHEMT with Fluorine Treatment," 2020 Device Research Conference (DRC), Jun. 2020.
4. **Ying-Ping Huang**, Chih-Chieh Huang, Ching-Sung Lee, and Wei-Chou Hsu, "High-Performance Normally-OFF AlGaN/GaN Fin-MISHEMT on Silicon With Low Work Function Metal-Source Contact Ledge," IEEE Trans. Electron Devices, vol. 67, no. 12, pp. 5434-5440, Dec. 2020.
5. Ching-Sung Lee, Xue-Cheng Yao, **Ying-Ping Huang**, and Wei-Chou Hsu, "Improved Ultraviolet Detection and Device Performance of Al_2O_3-Dielectric $In_{0.17}Al_{0.83}N$/ AlN/GaN MOS-HFETs," IEEE Journal of the Electron Devices Society, vol. 7, no. 1, pp. 430-434, Mar. 2019.
6. Ching-Sung Lee, Xue-Cheng Yao, **Ying-Ping Huang**, and Wei-Chou Hsu, "Al_2O_3-Dielectric InAlN/AlN/GaN Gamma-Gate MOS-HFETs With Composite Al_2O_3/TiO_2 Passivation Oxides," IEEE Journal of the Electron Devices Society, vol. 6, no. 1, pp. 1142-1146, Sep. 2018.
7. **Ying-Ping Huang**, Ching-Sung Lee, and Wei-Chou Hsu, "Novel Enhancement-Mode Tri-Gate InAlN/GaN Tunnel-Junction HEMT," 2020 International Conference on Solid State Devices and Materials (SSDM), Sep. 2020.
8. Ching-Sung Lee, Yan-Ting Shen, Wei-Chou Hsu, **Ying-Ping Huang**, and Cheng-Yang You, "$Al_{0.75}Ga_{0.25}N/Al_xGa_{1-x}N/Al_{0.75}Ga_{0.25}N$/AlN/SiC Metal-Oxide-Semiconductor Heterostructure Field-Effect Transistors With Symmetrically-Graded Widegap Channel," IEEE Journal of the Electron Devices Society, vol. 8, pp. 9-14, Nov. 2020.
9. Ching-Sung Lee, Wei-Chou Hsu, **Ying-Ping Huang**, Han-Yin Liu, and Wen-Luh Yang, "Comparative Study on Graded-Barrier $Al_xGa_{1-x}N$/AlN/GaN/Si Metal-Oxide-Semiconductor Heterostructure Field-Effect Transistor by Using Ultrasonic Spray Pyrolysis Deposition Technique," Semiconductor Science and Technology, vol. 33, no. 6, 065004, Jun. 2018.

指導教授　許渭州 特聘教授

現職　・國立成功大學 / 電資學院院長

學歷　・國立成功大學 / 電機博士

經歷　・國立成功大學 / 電資學院院長 (2015~now)
・國立成功大學 / 電資學院副院長 (2012~2015)
・國立成功大學 / 尖端光電中心主任 (2007~now)
・國立成功大學 / 電機工程學系系主任 (2005~2007)
・國立成功大學 / 特聘教授 (2002~now)

鄧名揚 Ming-Yang Deng

國立成功大學 電機工程學系

獲獎摘要

鄧名揚同學於 2016 年起於國立成功大學電機工程學系攻讀博士班。研究領域為基於薄膜電晶體之主動式矩陣顯示器系統電路設計，並針對高解析度及 Micro / Mini LED 等議題進行高驅動力及低功耗電路設計。相關成果已發表於TIE (1篇)、TED (2篇)、JEDS (3篇)、JDT (2篇) 等 IEEE 期刊上，並獲得10 項台灣專利。鄧同學於 2019 年學生獲得「科技部補助博士生赴國外研究」，以訪問學者身分前往美國中央佛羅里達大學進行Micro / Mini LED 之相關研究，其成果以共同第一作者身分發表論文於 Light：Science & Applications-Nature (2-year impact factor：14.240, over 36k accesses and 70 citations)。

得獎經歷

- 2020 年中華民國斐陶斐榮譽會員
- 2019 年潘文淵文教基金會獎學金
- 2019 年獲得「科技部補助博士生赴國外研究」補助十二個月
- 2018 年 SID 論文優秀獎
- 2017 年獲得友達光電第十四屆 A+ 暑期實習 - 第一名
- 2017 年”經濟部技術處搶鮮大賽”創意發想類 - 季軍
- 105 年度「科林科技論文獎」半導體與光電科技獎碩士組 - 優勝

重要學術著作 / 專利

1. **Ming-Yang Deng**, En-Lin Hsiang, Qian Yang, Chia-Ling Tsai, Bo-Shu Chen, Chia-En Wu, Ming-Hsien Lee, Shin-Tson Wu, and Chih-Lung Lin*, “Reducing Power Consumption of Active-Matrix Mini-LED Backlit LCDs by Driving Circuit,” IEEE Transactions on Electron Devices
2. Yuge Huang, En-Lin Hsiang, **Ming-Yang Deng**, and Shin-Tson Wu*, “Mini-LED, Micro-LED, and OLED Displays: Present Status and Future Perspectives,” Light: Science & Applications, 9.1: 1-16, 2020. These authors contributed equally: Yuge Huang, En-Lin Hsiang, **Ming-Yang Deng**
3. Chih-Lung Lin*, **Ming-Yang Deng**, Wen-Ching Chiu, Li-Wei Shih, Jui-Hung Chang, Yu-Sheng Lin, and Ching-En Lee, “A Pre-Bootstrapping Method for Use in Gate Driver Circuits to Improve the Scan Pulse Delay of High-Resolution TFT-LCD Systems,” IEEE Transactions on Industrial Electronics, vol. 67, no. 8, pp. 7015-7024, Aug. 2020.
4. **Ming-Yang Deng**, Wei-Sheng Liao, Sung-Chun Chen, Jui-Hung Chang, Chia-En Wu, and Chih-Lung Lin*, “Low-Leakage Capacitive Coupling Structure for a-Si:H Gate Driver with Less Delay of Clock Signals used in AMLCDs,” IEEE Journal of the Electron Devices Society, vol. 8, pp. 302-307, Mar. 2020.
5. Chih-Lung Lin*, Po-Syun Chen, **Ming-Yang Deng**, Chia-En Wu, Wen-Ching Chiu, and Yu-Sheng Lin, “UHD AMOLED Driving Scheme of Compensation Pixel and Gate Driver Circuits Achieving High-Speed Operation,” IEEE Journal of the Electron Devices Society, vol. 6, pp. 26-33, Dec. 2017.
6. Chih-Lung Lin*, **Ming-Yang Deng**, Chia-En Wu, Chih-Cheng Hsu, and Chia-Lun Lee, “Hydrogenated Amorphous Silicon Gate Driver with Low-Leakage for Thin-Film Transistor Liquid Crystal Display Applications,” IEEE Transactions on Electron Devices, vol. 64, no. 8, pp. 3193-3198, Aug. 2017.
7. Chih-Lung Lin*, **Ming-Yang Deng**, Chia-En Wu, Po-Syun Chen, and Ming-Xun Wang, “Gate Driver Circuit Using Pre-Charge Structure and Time-Division Multiplexing Driving Scheme for Active-Matrix LCDs Integrated with In-Cell Touch Structures,” IEEE/OSA Journal of Display Technology, vol. 12, no. 11, pp. 1238-1241, Nov. 2016.
8. 林志隆，**鄧名揚**，林祐陞，陳柏澍，林捷安，吳佳恩，李明賢，彭佳添，“畫素驅動電路” I718909. 2021
9. 林志隆，**鄧名揚**，林祐陞，廖威勝，吳佳恩，李明賢，彭佳添，“畫素驅動電路” I712026. 2020
10. 林志隆，**鄧名揚**，陳柏勳，賴柏君，鄭貿薰，“顯示面板” I683296. 2020

指導教授　林志隆 特聘教授

現職　・國立成功大學 / 電機工程學系教授兼系主任

學歷　・國立台灣大學 / 電機工程學系博士

經歷　・國立成功大學 / 電機工程學系系主任 (2020~)

・中華民國光電學會 (TPS) / 秘書長 (2020~)

・國立成功大學 / 電機工程學系副系主任 (2017~2020)

・台灣顯示器產業聯合總會 (TDUA) / 理事 (2017)

・科技部 / 工程中心企劃組組長 (2014~2016)

・國立台灣大學 / 電機系助教 (1993/8~1999/7)

戴茂洲 Mao-Chou Tai

國立中山大學 光電工程研究所

獲獎摘要

戴茂洲同學自 2019 年起於國立中山大學光電工程研究所攻讀博士班，博士班期間專注於金屬氧化物半導體場效電晶體 (Metal-Oxide-Semiconductor Field-Effect Transistors) 的可靠度物理機制探討和記憶體 (Memory) 相關應用開發。在釐清各式元件的可靠度議題後，藉由產學合作提出有效的結構或製程改善方法，迄今已獲證 1 項台灣專利與 1 項美國專利 (3 項台美專利申請中)。除此之外，優異的研究成果使其目前以第一作者共發表 7 篇 SCI 國際期刊包含 Advanced Electronics Materials / IEEE Electronic Device Letters / Applied Physics Letters 等國際期刊。

得獎經歷

- 國立中山大學創新育成中心 - 貨櫃創業計畫進駐團隊：『Ocean Crystal』
- 國防工業獎學金
- 日月光集團獎學金

重要學術著作

1. **M.-C. Tai**, Y.-X. Wang, T.-C. Chang*, et. al, “Heterojunction Channels in Oxide Semiconductors for Visible-Blind Nonvolatile Optoelectronic Memories” Advanced Electronic Materials, 6, 11, 2000747, 2020.
2. **M.-C. Tai**, Y.-X. Wang, T.-C. Chang*, et. al, “Gate Dielectric Breakdown in a-InGaZnO Thin Film Transistors with Cu Electrodes” IEEE Electron Device Letters, 42, 6, 851-854, 2021.
3. **M.-C. Tai**, T.-C. Chang*, M.-C. Chen, et. al, “Floating top gate-induced output enhancement of a-InGaZnO thin film transistors under single gate operations,” Applied Physics Letters, vol. 113, no. 17, pp. 173501, 2018.
4. **M.-C. Tai**, Y.-C. Tsao, Y.-X. Wang, C.-C. Lin, Y.-L. Tsai, H.-Y. Tu, B.-S. Huang, T.-C. Chang, “Dynamic Switching-Induced Back Carrier Injection in a-InGaZnO Thin Film Transistors,” Journal of Physics D: Applied Physics, 54, 2, 025111, 2020.
5. **M.-C. Tai**, P.-W. Chang, T.-C. Chang*, et. al, “Effect of a-InGaZnO TFTs' Channel Thickness under Self-Heating Stress,” ECS Journal of Solid State Science and Technology, 8 (10), Q185-Q188 2019.
6. C.C. Lin, **M.-C. Tai** (contributed equally in this work), T.-C. Chang, et. al, “Interface Defect Shielding of Electron Trapping in a-InGaZnO Thin Film Transistors” IEEE Transactions on Electron Devices, 67, 9, 3645-3649, 2020.
7. Y.-X. Wang, **M.-C. Tai** (contributed equally in this work), T.-C. Chang, et. al, “Suppression of Edge Effect Induced by Positive Gate Bias Stress in Low-Temperature Polycrystalline Silicon TFTs with Channel Width Extension Over Source/Drain Regions” IEEE Transactions on Electron Devices, 67, 12, 5552-5556, 2020.
8. T.-C. Chang, Y.-C- Tsao, P.-H. Chen, **M.-C. Tai**, et. al, “Flexible Low-Temperature Polycrystalline Silicon Thin-Film Transistors” Materials Today Advance (5), 100040, 2020. – Review Article
9. Y.-X. Wang, S.-P. Huang, **M.-C. Tai**, et. al, “A Novel Structure Serving as a Stress Relief Layer for Flexible LTPS TFTs”, 2019 IEEE International Electron Device Meetings (IEEE IEDM), San Francisco, CA, USA
10. **M.-C. Tai**, P.-W. Chang, T.-C. Chang, et. al, “Effect of Different a-InGaZnO TFTs' Channel Thickness upon Self-Heating Stress” 2019 Semiconductor Technology for Ultra Large Scale Integrated Circuits and Thin Film Transistors VII, Kyoto, Japan

指導教授　張鼎張 講座教授

現職　・國立中山大學 / 物理系
學歷　・國立交通大學 / 電子所博士
經歷　・ IEEE Fellow
・國立中山大學物理系 / 講座教授
・國家奈米實驗室研究員
・有庠科技講座