獎項介紹

「TSIA 半導體獎」是台灣半導體產業協會於 2014 年起，為了獎勵國內積極從事半導體之學術研究、發明或致力投入產業合作並有具體貢獻者而設立。

此獎項之得獎人由本會遴選委員會評選，遴選委員由在半導體領域已有卓越成就之學者、專家及產業領導者擔任。

今年具博士學位之新進研究人員半導體獎由台灣大學白奇峰助理教授獲獎；博士研究生半導體獎得獎者，分別由台大、交大、成大、清大、中山等校 11 位博士班同學獲獎，本會期許得獎人以成為台灣半導體產業優秀貢獻者為目標，再接再厲，為台灣半導體產業之永續發展而戮力前進。

贊助單位：理監事公司

力成科技股份有限公司	力晶科技股份有限公司	力晶積成電子製造股份有限公司
工業技術研究院	日月光半導體製造股份有限公司	世界先進積體電路股份有限公司
立錡科技股份有限公司	台灣積體電路製造股份有限公司	欣銓科技股份有限公司
矽品精密工業股份有限公司	南亞科技股份有限公司	凌陽科技股份有限公司
創意電子股份有限公司	華邦電子股份有限公司	鈺創科技股份有限公司
漢民科技股份有限公司	聯發科技股份有限公司	聯華電子股份有限公司

◎ 以上依公司筆劃順序排列

白奇峰 Chi-Feng Pai

國立台灣大學 材料科學與工程學系

獲獎摘要

白奇峰博士於研究所期間進入自旋電子學領域，致力於研究材料中之自旋霍爾效應 (spin Hall effect)，成功開發自旋霍爾效應材料與磁穿隧節 (magnetic tunnel junction) 之結合元件，發明自旋軌道矩磁性記憶體 (spin-orbit torque MRAM)。相關研究成果除了獲得美國專利，至今已有共超過 5,000 次之引用。近年來，在學術研究以外，也與工研院電光系統所及台灣積體電路公司合作，希望將自旋軌道矩記憶體的技術轉移至台灣業界。另外，較接近實際應用的 MRAM 相關課題，白博士的團隊在近年也開始研究新穎材料系統，如拓樸絕緣體 (topological insulators)，探討拓樸絕緣體在磁記憶體及半導體產業中可能之應用，與將面臨之挑戰。

得獎經歷

- 2019 科技部年輕學者計畫 (哥倫布計畫)
- 2017 工業技術研究院傑出研究獎
- 2016 AUMS (Asian Union of Magnetics Societies) Young Researcher Award

重要學術著作

1. Tian-Yue Chen, Cheng-Wei Peng, Tsung-Yu Tsai, Wei-Bang Liao, Chun-Te Wu, Hung-Wei Yen, and **Chi-Feng Pai***, Efficient Spin-Orbit Torque Switching with Nonepitaxial Chalcogenide Heterostructures (2020, Jan). ACS Appl. Mater. Interfaces 12, 7788.
2. **Chi-Feng Pai***, Switching by Topological Insulators (2018, Jul). Nature Materials, 17, 755.
3. Ting-Chien Wang, Tian-Yue Chen*, Chun-Te Wu, Hung-Wei Yen, and **Chi-Feng Pai***, A Comparative Study on Spin-Orbit Torque Efficiencies from W/ferromagnetic and W/ferrimagnetic Heterostructures (2018, Jan). Physical Review Materials, 2, 014403.
4. Tian-Yue Chen, Tsao-Chi Chuang, Ssu-Yen Huang, Hung-Wei Yen, **Chi-Feng Pai***, Spin-orbit torque from a magnetic heterostructure of high-entropy alloy (2017, Oct). Physical Review Applied, 8, 044005.
5. Tian-Yue Chen, Hsin-I Chan, Wei-Bang Liao, and **Chi-Feng Pai***, Current-induced spin-orbit torque and field-free switching from Mo-based magnetic heterostructures (2018, Oct). Physical Review Applied 10, 044038.
6. **Chi-Feng Pai***, Maxwell Mann, Aik Jun Tan, Geoffrey S. D. Beach* (2016, Apr). Determination of spin torque efficiencies in heterostructures with perpendicular magnetic anisotropy. Physical Review B, 93, 144409.
7. Can Onur Avci, Andy Quindeau, **Chi-Feng Pai**, Maxwell Mann, Lucas Caretta, Astera Tang, Mehmet Onbasli, Caroline Ross*, Geoffrey Beach* (2016, Nov). Current-Induced Switching in a Magnetic Insulator. Nature Materials, 16, 309.
8. Tian-Yue Chen, Tsao-Chi Chuang, Ssu-Yen Huang, Hung-Wei Yen, **Chi-Feng Pai*** (2017, Oct). Spin-orbit torque from a magnetic heterostructure of high-entropy alloy. Physical Review Applied, 8, 044005.
9. Luqiao Liu†, **Chi-Feng Pai**†, Y. Li, H. W. Tseng, D. C. Ralph, and R. A. Buhrman* (2012, May). Spin-Torque Switching with the Giant Spin Hall Effect of Tantalum. Science, 336, 555-558.
10. **Chi-Feng Pai***, Luqiao Liu, Y. Li, H. W. Tseng, D. C. Ralph, R. A. Buhrman (2012, Sep). Spin transfer torque devices utilizing the giant spin Hall effect of tungsten. Applied Physics Letters, 101, 122404.

指導教授

Prof. Robert A. Buhrman

現職　John Edson Sweet Memorial Professor of Engineering, School of Applied and Engineering Physics, Cornell University

學歷　Ph.D. in Applied Physics, Cornell University

經歷　・American Academy of Arts and Sciences (AAAS) Fellow, American Physical Society (APS) Fellow, Senior Vice Provost for Research of Cornell University

推薦專家

謝宗霖 教授員

現職　國立台灣大學 / 材料科學與工程學系教授兼系主任

學歷　Ph.D. in Materials Science and Engineering, University of Cambridge

經歷　・台灣大學材料系教授
・國科會工程處優秀年輕學者
・陶業研究學會優秀青年會員

TSIA 2020 半導體獎

博 士 研 究 生

王韋程 Wei-Chen Wang

國立台灣大學 資訊工程學研究所

獲獎摘要

王韋程同學自 2017 年起於國立台灣大學資訊工程學研究所攻讀博士班。研究領域包含新興非揮發性記憶體、嵌入式系統與記憶體 / 儲存系統。曾於 IEEE TCAD 與 ACM TECS 等頂尖國際期刊，以及 CODES+ISSS、ICCAD 等 ACM / IEEE 頂尖國際會議中發表論文。此外，於 2019 年 10 月在美國紐約市舉辦的嵌入式系統領域國際頂尖研討會 ACM / IEEE CODES+ISSS 中，其研究成果被評選為年度最佳論文獎，為該會議 28 年來首次由台灣研究團隊獲獎。王同學於研究領域成果豐碩，難能可貴。

得獎經歷 / 專利

- 2019 榮獲財團法人潘文淵文教基金會獎學金
- 2019 榮獲 ACM / IEEE International Conference on Hardware / Software Codesign and System Synthesis (CODES+ISSS) 最佳論文獎
- “記憶體系統以及記憶體操作方法”，中華民國發明專利公告第 I694449 號
- “記憶體裝置及應用於其上之資料管理方法”，中華民國發明專利公告第 I629592 號
- 2015 代表國立台灣大學團隊於 ACM KDD Cup 全球 821 隊中榮獲第四名

重要學術著作

1. **Wei-Chen Wang**, Chien-Chung Ho, Yu-Ming Chang, and Yuan-Hao Chang, “Challenges and Designs for Secure Deletion in Storage Systems," IEEE International Conference on Computing, Analytics and Networks (ICAN), Chiayi, Taiwan, Feb. 7-8, 2020.
2. **Wei-Chen Wang**, Ping-Hsien Lin, Yung-Chun Li, Chien-Chung Ho, Yu-Ming Chang, and Yuan-Hao Chang, "Toward Instantaneous Sanitization through Disturbance-induced Errors and Recycling Programming over 3D Flash Memory," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), Westminster, CO, USA, Nov. 4 – Nov. 7, 2019. (Top Conference)
3. **Wei-Chen Wang**, Yuan-Hao Chang, Tei-Wei Kuo, Chien-Chung Ho, Yu-Ming Chang, and Hung-Sheng Chang, "Achieving Lossless Accuracy with Lossy Programming for Efficient Neural-Network Training on NVM-Based Systems," ACM Transactions on Embedded Computing Systems (TECS), vol. 18, Issue 5s, no. 68, pp. 68:1-68:22, Oct. 2019. (Integrated with ACM/IEEE CODES+ISSS'19) (Best Paper Award - Top Conference)
4. Ping-Hsien Lin, Yu-Ming Chang, Yung-Chun Li, **Wei-Chen Wang**, Chien-Chung Ho, and Yuan-Hao Chang, "Achieving Fast Sanitization with Zero Live Data Copy for MLC Flash Memory," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), San Diego, California, USA, Nov. 5-8, 2018. (Top Conference)
5. **Wei-Chen Wang**, Chien-Chung Ho, Yuan-Hao Chang, Tei-Wei Kuo, and Ping-Hsien Lin, "Scrubbing-aware Secure Deletion for 3D NAND Flash," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 37, no. 11, pp. 2790-2801, Nov. 2018. (Integrated with ACM/IEEE CODES+ISSS'18) (Top Conference)
6. Chien-Chung Ho, Yung-Chun Li, Ping-Hsien Lin, **Wei-Chen Wang**, and Yuan-Hao Chang, "A Stride-away Programming Scheme to Resolve Crash Recoverability and Data Readability Issues of Multi-level-cell Flash Memory," IEEE Nonvolatile Memory Systems and Applications Symposium (NVMSA), Hakodate, Japan, Aug. 28-31, 2018.

指導教授

郭大維 教授

現職　・國立台灣大學 / 資訊工程學系特聘教授
　　・香港城市大學 / 李兆基資訊工程講座教授、校長資深顧問暨工學院院長

學歷　美國德州大學奧斯汀分校 / 電腦科學博士

經歷　・國立台灣大學 / 代理校長
　　・國立台灣大學 / 學術副校長
　　・美國計算機協會會士 ACM Fellow
　　・國際電機電子工程師學會會士 IEEE Fellow
　　・美國發明家學院院士 NAI Fellow

共同指導教授

張原豪 研究員

現職　中央研究院 / 資訊科學研究所

學歷　國立台灣大學 / 資訊工程博士

經歷　・中央研究院 / 資訊科學研究所副所長
　　・中央研究院 / 資訊科學研究所研究員

TSIA 2020 半導體獎

博 士 研 究 生

呂芳諒 Fang-Liang Lu

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獲獎摘要

呂芳諒同學於博士班就讀期間專注於四族磊晶技術開發、高摻雜磊晶層與低金屬半導體接觸電阻應用，其成長之磊晶結構擁有高元件表現，摻雜活化濃度與接觸電阻在 N 型與 P 型鍺基材料中皆為國際一流水準，相關研究成果發表於 IEEE 頂尖國際會 IEDM 與 Symp. VLSI 和一流之 IEEE 期刊。成果豐碩，難能可貴。

得獎經歷

- 2019 Outstanding Student Award of Graduate Institute of Electronics Engineering, National Taiwan University (2019 國立台灣大學電子工程學研究所學生傑出研究獎)
- 2018 Outstanding Youth of The Electronics Devices and Materials Association (2018 台灣電子材料與元件協會傑出青年獎)
- 2015 22nd SNDT (Symposium on Nano Device Technology) Best Student Paper (2015 第 22 屆 SNDT 學生論文頭等獎)
- 2014 Best Student Paper at 1st place of tsmc-NTU Research Center (2014 台積電 - 台灣大學聯合研發中心論文競賽首獎)

重要學術著作

1. **Fang-Liang Lu**, Yi-Chun Liu, Chung-En Tsai, Hung-Yu Ye, and C. W. Liu, "Record Low Contact Resistivity to Ge:B ($8.1\times10^{-10}\Omega$-cm^2) and GeSn:B ($4.1\times10^{-10}\Omega$-cm^2) with Optimized [B] and [Sn] by In-situ CVD Doping," in Symposia on VLSI Technology and Circuits (VLSI), Jun. 2020.
2. Yu-Shiang Huang, **Fang-Liang Lu**, Chien-Te Tu, Jyun-Yan Chen, Chung-En Tsai, Hung-Yu Ye, Yi-Chun Liu and C. W. Liu, "First Demonstration of 4-Stacked $Ge_{0.915}Sn_{0.085}$ Wide Nanosheets by Highly Selective Isotropic Dry Etching with High S/D Doping and Undoped Channels," in Symposia on VLSI Technology and Circuits (VLSI), Jun. 2020.
3. Chien-Te Tu, Yu-Shiang Huang, **Fang-Liang Lu**, Hsiao-Hsuan Liu, Chung-Yi Lin, Yi-Chun Liu, and C. W. Liu, "First Vertically Stacked Tensily Strained $Ge_{0.98}Si_{0.02}$ nGAAFETs with No Parasitic Channel and L_G = 40 nm Featuring Record I_{ON} = 48 μA at V_{OV}=V_{DS}=0.5V and Record $G_{m,max}$(μS/μm)/SS_{SAT}(mV/dec) = 8.3 at V_{DS}=0.5V," in International Electron Devices Meeting (IEDM), Dec. 2019.
4. **Fang-Liang Lu**, Chung-En Tsai, Chih-Hsiung Huang, Hung-Yu Ye, Shih-Ya Lin, C. W. Liu, "Record Low Contact Resistivity ($4.4\times10^{-10}\Omega$-cm^2) to Ge Using In-situ B and Sn Incorporation by CVD With Low Thermal Budget (≤400℃) and Without Ga," in Symposia on VLSI Technology and Circuits (VLSI), Jun. 2019.
5. Yu-Shiang Huang, **Fang-Liang Lu**, Ya-Jui Tsou, Hung-Yu Ye, Shih-Ya Lin, Wen-Hung Huang, and C. W. Liu, "Vertically Stacked Strained 3-GeSn-Nanosheet pGAAFETs on Si Using GeSn/Ge CVD Epitaxial Growth and the Optimum Selective Channel Release Process," IEEE Electron Device Letters, Vol. 39, No. 9, pp. 1274-1277, Sep. 2018.
6. **Fang-Liang Lu**, Chung-En Tsai, I-Hsieh Wong, Chun-Ti Lu, and C. W. Liu, "Dopant Recovery in Epitaxial Ge on SOI by Laser Annealing With Device Applications," IEEE Transactions on Electron Devices, Vol. 65, No. 7, pp. 2925-2931, Jul. 2018.
7. Yu-Shiang Huang, **Fang-Liang Lu**, Ya-Jui Tsou, Chung-En Tsai, Chung-Yi Lin, Chih-Hao Huang, and C. W. Liu, "First Vertically Stacked GeSn Nanowire pGAAFETs with I_{on}=1850μA/μm (V_{OV}=V_{DS}=-1V) on Si by GeSn/Ge CVD Epitaxial Growth and Optimum Selective Etching," in International Electron Devices Meeting (IEDM), Dec. 2017.
8. I-Hsieh Wong, **Fang-Liang Lu**, Shih-Hsien Huang, Hung-Yu Ye, Chun-Ti Lu, Jhih-Yang Yan, Yu-Cheng Shen, Yu-Jiun Peng, Huang-Siang Lan, and C. W. Liu, "High Performance Ge Junctionless Gate-all-around NFETs with Simultaneous I_{on} =1235 μA/μm at V_{OV}=V_{DS}=1V, SS=95 mV/dec, high I_{on}/I_{off}=2E6, and Reduced Noise Power Density using S/D Dopant Recovery by Selective Laser Annealing," in International Electron Devices Meeting (IEDM), Dec. 2016.
9. Yu-Shiang Huang, Chih-Hsiung Huang, **Fang-Liang Lu**, Chung-Yi Lin, Hung-Yu Ye, I-Hsieh Wong, Sun-Rong Jan, Huang-Siang Lan, C. W. Liu, Yi-Chiau Huang, Hua Chung, Chorng-Ping Chang, Schubert S. Chu, and Satheesh Kuppurao "Record High Mobility (428cm^2/V-s) of CVD-grown Ge/Strained $Ge_{0.91}Sn_{0.09}$/Ge Quantum Well p-MOSFETs," in International Electron Devices Meeting (IEDM), Dec. 2016.
10. S.-H. Huang, **F.-L. Lu**, W.-L. Huang, C.-H. Huang, and C. W. Liu, "The ~ 3×10^{20} cm^{-3} Electron Concentration and Low Specific Contact Resistivity of Phosphorus-Doped Ge on Si by In-situ Chemical Vapor Deposition Doping and Laser Annealing," IEEE Electron Device Letter, Vol. 36, No. 11, pp. 1114-1117, Nov. 2015.

指導教授

劉致為 教授

現職 Distinguished / Chair Professor, National Taiwan University
IEEE Fellow

學歷
- Ph.D. 1994 Electrical Engineering, Princeton University
- MS.1987 and B.S. 1985, National Taiwan University, Taiwan

經歷
- Deputy General Director (副主任 , 2008 ~ 2013) / Senior full researcher (資深研究員 , 2011~), National Nano Device Labs
- Research Director / Senior full researcher (資深研究員), ERSO / ITRI (2002 ~ 2005)

鍾嘉哲 Chia-Che Chung

國立台灣大學 電子工程學研究所

獲獎摘要

鍾嘉哲於博士班就讀期間專注於三維電晶體在元件與電路層級的自發熱效應模擬，建立 SPICE 熱模型與類神經網路來模擬鰭式電晶體在電路內的溫度分佈，以及用 TCAD 模擬堆疊矽通道閘極環繞式電晶體內的通道間溫差與所致的臨界電壓差。相關結果發表於 2020 VLSI 等頂尖國際會議，與 EDL、TED 等一流之 IEEE 期刊。成果豐碩，難能可貴。

得獎經歷

- tsmc-NTU Undergraduate Competition Award, 1st Price (台積電台大聯合研發中心 大學部「專題研究競賽」第一名)
- tsmc-Top 4 University Research Award, 2nd Price (台積電四校聯合研發中心 大學部「專題研究競賽」第二名)
- NTU Innovation Award (第十五屆台大創新競賽特別獎 " 可行性獎 ")

重要學術著作

1. **Chia-Che Chung**, Hsin-Cheng Lin, H. H. Lin, W. K. Wan, M.-T. Yang, and C. W. Liu, "Interpretable Neural Network to Model and to Reduce Self-Heating of FinFET Circuitry," Symposia on VLSI Technology and Circuits (VLSI), Honolulu, HI, Jun. 14-19, 2020.
2. **Chia-Che Chung**, Hung-Yu Ye, H. H. Lin, W. K. Wan, M.-T. Yang, and C. W. Liu, "Self-Heating Induced Interchannel V_t Difference of Vertically Stacked Si Nanosheet Gate-All-Around MOSFETs," IEEE Electron Device Letters, vol. 40, no. 12, pp. 1913-1916, Dec. 2019.
3. **Chia-Che Chung**, H. H. Lin, W. K. Wan, M.-T. Yang, and C. W. Liu, "Thermal SPICE Modeling of FinFET and BEOL Considering Frequency-Dependent Transient Response, 3-D Heat Flow, Boundary/Alloy Scattering, and Interfacial Thermal Resistance," IEEE Transactions on Electron Devices, Vol. 66, No. 6, pp. 2710-2714, Jun. 2019.
4. (invited) **Chia-Che Chung** and C. W. Liu, "FinFET Thermal Modeling and Circuit Thermal Simulation," JST-MOST Joint Workshop, Kyoto, Japan, Jun. 14, 2019.
5. (invited) **Chia-Che Chung**, Hsin-Cheng Lin, H. H. Lin, Y. H. Huang, M.-T. Yang, and C. W. Liu, "Thermal Simulation of FinFET Circuit," The 31st VLSI Design/CAD Symposium (VLSI/CAD), Taichung, Aug. 4-7, 2020.
6. Jhih-Yang Yan, **Chia-Che Chung**, Sun-Rong Jan, H. H. Lin, W. K. Wan, M.-T. Yang, and C. W. Liu, "Comprehensive Thermal SPICE Modeling of FinFETs and BEOL with Layout Flexibility Considering Frequency Dependent Thermal Time Constant, 3D Heat Flows, Boundary/Alloy Scattering, and Interfacial Thermal Resistance with Circuit Level Reliability Evaluation," Symposium on VLSI Technology and Circuits (VLSI), Honolulu, HI, 2018.
7. Hung-Yu Ye, **Chia-Che Chung**, and C. W. Liu, "Mobility Calculation of Ge Nanowire Junctionless and Inversion-Mode Nanowire NFETs with Size and Shape Dependence," IEEE Transactions on Electron Devices, vol. 65, no. 12, pp. 5295-5300, Dec. 2018.
8. Hung-Yu Ye, **Chia-Che Chung**, I-Hsieh Wong, Huang-Siang Lan, and C. W. Liu, "Mobility Calculation of Ge Nanowire Junctionless NFETs with Size and Geometry Dependence," 2018 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), Hsinchu, Apr. 16-19, 2018.
9. Ya-Jui Tsou, **Chia-Che Chung**, Jih-Chao Chiu, Huan-Chi Shih, and C. W. Liu, "Thermal and Reliability Modeling of FinFET-Driven STT-pMTJ Array Considering Mutual Coupling, 3D Heat Flow, and BEOL Effects," IEDM MRAM Poster, 2019.
10. Hung-Yu Ye, **Chia-Che Chung**, and C. W. Liu, "Electron Mobility Enhancement by Tensile Strain in Germanium Nanowire NFETs Considering Surface Roughness, Channel Dopant Charge, Interface Charge, and Phonon Scattering," 49th IEEE Semiconductor Interface Specialists Conference (SISC), San Diego, CA, Dec. 5-8, 2018.

指導教授

劉致為 教授

現職　Distinguished / Chair Professor, National Taiwan University
IEEE Fellow

學歷
- Ph.D. 1994 Electrical Engineering, Princeton University
- MS.1987 and B.S. 1985, National Taiwan University, Taiwan

經歷
- Deputy General Director (副主任 , 2008 ~ 2013) / Senior full researcher (資深研究員 , 2011~), National Nano Device Labs
- Research Director / Senior full researcher (資深研究員), ERSO / ITRI (2002 ~ 2005)

張祖齊 Tsu-Chi Chang

國立交通大學 光電工程研究所

獲獎摘要

張祖齊同學於國立交通大學光電工程研究所攻讀博士班，研究領域為垂直共振腔面射型雷射 (Vertical Cavity Surface Emitting Lasers, VCSELs) 與高折射率差光柵 (High-Index-Contrast Grating, HCG) 元件設計製作。並與瑞典查默斯理工大學進行國際研究合作，製作出世界第一顆電激發高折射率差光柵氮化鎵垂直共振腔面射型雷射，讓藍光 VCSEL 發展多了另一種可能性。曾於 SPIE Photonics West、MOC、PIERS 等頂尖國際會議中報告 GaN VCSEL 與 HCG VCSELs 相關研究；其研究成果也發表於 ACS Photonics、Scientific Reports 等國際頂尖期刊，並登上 ACS Photonics 期刊封面；其元件設計於 2019 年 9 月獲得專利許可。張同學在博士班期間除了有國際研究合作經驗，且研究成果豐碩，獲得此獎實至名歸。

得獎經歷 / 專利

- 「具有混合式反射鏡結構的垂直共振腔面射型雷射」，2019 年 9 月核准，中華民國專利第 I676327 號。
- 應用單石整合之高折射率差光柵於氮化鎵垂直共振腔面射型雷，2019 晶元光電，晶鷹盃科技競賽，理論概念組，發光獎。
- 2018 南亞科技獎學金。
- GaN-based vertical-cavity surface-emitting lasers operating at high temperature, 22th MicroOptics Conference, 2017 MOC Student Award. (Speaker)

重要學術著作與專利

1. **Tsu-Chi Chang**, Ehsan Hashemi, Kuo-Bin Hong, Jörgen Bengtsson, Johan Gustavsson, Åsa Haglund and Tien-Chang Lu, “Electrically Injected GaN-Based Vertical-Cavity Surface-Emitting Lasers with TiO2 High-Index-Contrast Grating Reflectors,” ACS Photonics, 7, 861-866 (2020).
2. **Tsu-Chi Chang**, Kuo-Bin Hong, Shuo-Yi Kuo, Tien-Chang Lu, Demonstration of polarization control GaN-based micro-cavity lasers using a rigid high-contrast grating reflector. Scientific reports, 9, 1-6 (2019).
3. Chia-Yen Huang, Tzu-Ying Tai, Jing-Jie Lin, **Tsu-Chi Chang**, Che-Yu Liu, Tien-Chang Lu, Yuh-Renn Wu, and Hao-Chung Kuo, “Mode-hopping phenomena in the InGaN-based core–shell nanorod array collective lasing.” ACS Photonics, 5, 2724-2729 (2018).
4. Yu-Hsun Chou , Kuo-Bin Hong, Chun-Tse Chang, **Tsu-Chi Chang**, Zhen-Ting Huang, Pi-Ju Cheng, Jhen-Hong Yang, Meng-Hsien Lin, Tzy-Rong Lin, Kuo-Ping Chen , Shangjr Gwo, and Tien-Chang Lu, “Ultracompact pseudowedge plasmonic lasers and laser arrays.” Nano letters, 18, 747-753 (2018).
5. Kou-Bin Hong, Chun-Yan Lin, **Tsu-Chi Chang**, Wei-Hsuan Liang, Ying-Yu Lai, Chien-Ming Wu, You-Lin Chuang, Tien-Chang Lu, Claudio Conti, and Ray-Kuang Lee, “Lasing on nonlinear localized waves in curved geometry.” Optics Express, 25, 29068-29077 (2017).
6. **Tsu-Chi Chang**, Shiou-Yi Kuo, Jhen-Ting Lian, Kuo-Bin Hong, Shing-Chung Wang and Tien-Chang, “High-temperature operation of GaN-based vertical-cavity surface-emitting lasers.” Applied Physics Express, 10, 112101 (2017).
7. Chia-Yen Huang, Jing-Jie Lin, **Tsu-Chi Chang**, Che-Yu Liu, Tzu-Ying Tai, Kuo-Bin Hong, Tien-Chang Lu, and Hao-Chung Kuo, “Collective lasing behavior of monolithic GaN-InGaN core–shell nanorod lattice under room temperature.” Nano letters, 17, 6228-6234 (2017).
8. Ying-Yu Lai, **Tsu-Chi Chang**, Ya-Chen Li, Tien-Chang Lu, and Shing-Chung Wang, “Electrically Pumped III-N Microcavity Light Emitters Incorporating an Oxide Confinement Aperture.” Nanoscale research letters, 12, 15 (2017).
9. **Tsu-Chi Chang**, Kuo-Bin Hong, Ying-Yu Lai, Yu-Hsun Chou, Shing-Chung Wang and Tien-Chang Lu, “ZnO-based microcavities sculpted by focus ion beam milling.” Nanoscale research letters, 11, 319 (2016).

指導教授

盧廷昌 特聘教授

現職　國立交通大學 / 光電工程學系系主任

學歷　・國立台灣大學 / 光電工程研究所博士
　　・美國南加州大學 / 電機工程研究所碩士

經歷　・友嘉光電 / 磊晶部經理 (2004 ~ 2005)
　　・國立交通大學 / 光電工程學系教授 (2005~)
　　・田家炳光電中心主任 (2018~)

黃陳嵩文 Sung-Wen Huang Chen　國立交通大學 光電工程研究所

獲獎摘要

黃陳嵩文同學於 2016 年起於國立交通大學光電工程研究所攻讀博士班。研究領域為奈米結構與半極化微型發光二極體應用。至今累積發表國際期刊 10 餘篇，國際研討會議論文 5 篇，論文代表作「Full-color monolithic hybrid quantum dot nanoring micro light-emitting diodes with improved efficiency using atomic layer deposition and nonradiative resonant energy transfer」更被選為頂尖國際光電期刊 Photonics Research 期刊封面以及 2019 年該期刊引用數前十名，表示黃陳同學的研究成果對該領域具有相當的貢獻。

得獎經歷

- 2020 年 晶元光電晶鷹盃科技競賽，理論概念組，第二名。
- 2019 年 科技部未來科技突破獎。
- 2019 年 財團法人中技社研究獎學金。
- 2019 年 晶元光電晶鷹盃科技競賽，理念概念組，第一名。
- 2019 年 EITA 新興材料研討會，最佳論文獎。

重要學術著作

1. **Sung-Wen Huang Chen**, Y.-M. Huang, Y.-H. Chang, Y. Lin, F.-J. Liou, Y.-C. Hsu, J. Song, J. Choi, C.-W. Chow, C.-C. Lin, R.-H. Horng, Z. Chen, J. Han, T. Wu, and H.-C. Kuo, "High-bandwidth green semipolar (20-21) InGaN/GaN micro light-emitting diodes for visible light communication," Accepted by ACS photonics, 2020.
2. **Sung-Wen Huang Chen**, Y.-M. Huang, K. J. Singh, Y.-C. Hsu, F.-J. Liou, J. Song, J. Choi, P.-T. Lee, C.-C. Lin, Z. Chen, J. Han, T. Wu, and H.-C. Kuo, "Full-color micro-LED display with high color stability using semipolar (20-21) InGaN LEDs and quantum-dot photoresist," Photonics Research, vol. 8, no. 5, pp. 630-636, 2020.
3. **Sung-Wen Huang Chen**, C.-C. Shen, T.-Z. Wu, Z.-Y. Liao, L.-F. Chen, J.-R. Zhou, C.-F. Lee, C.-H. Lin, C.-C. Lin, C.-W. Sher, P.-T. Lee, A.-J. Tzou, Z. Chen, and H.-C. Kuo, "Full-color monolithic hybrid quantum dot nanoring micro light-emitting diodes with improved efficiency using atomic layer deposition and nonradiative resonant energy transfer," Photonics Research, vol. 7, no. 4, pp. 416-422, 2019.
4. **Sung-Wen Huang Chen**, S.-W. Wang, K.-B. Hong, H. Medin, C.-H. Chung, C.-C. Wu, T.-Y. Su, F.-I. Lai, P.-T. Lee, S.-Y. Kuo, H.-C. Kuo, and Y.-L. Chueh, "Enhanced wavelength-selective photoresponsivity with a MoS_2 bilayer grown conformally on a patterned sapphire substrate," Journal of Materials Chemistry C, vol. 7, no. 6, pp. 1622-1629, 2019.
5. X. Jia, **Sung-Wen Huang Chen**, Y.-J. Liu, X. Hou, Y.-H. Zhang, Z.-H. Zhang, and H.-C. Kuo, "Design strategies for mesa-type gan-based schottky barrier diodes for obtaining high breakdown voltage and low leakage current," IEEE Transactions on Electron Devices, vol. 67, no. 5, pp. 1931-1938. 2020.
6. Z.-H. Zhang, **Sung-Wen Huang Chen**, Y.-H. Zhang, L.-P. Li, S.-W. Wang, K.-K. Tian, C.-S. Chu, M.-Q. Fang, H.-C. Kuo, and W.-A. Bi, "Hole transport manipulation to improve the hole injection for deep ultraviolet light-emitting diodes," ACS Photonics, vol. 4, no. 7, pp. 1846-1850, 2017.
7. Z.-H. Zhang, **Sung-Wen Huang Chen**, C.-S. Chu, K.-K. Tian, M.-Q. Fang, Y.-H. Zhang, W.-G. Bi, and H.-C. Kuo, "Nearly efficiency-droop-free AlGaN-based ultraviolet light-emitting diodes with a specifically designed superlattice p-type electron blocking layer for high mg doping efficiency," Nanoscale research letters, vol. 13, no. 1, p. 122, 2018.
8. J.-Q. Kou, **Sung-Wen Huang Chen**, J.-M. Che, H. Shao, C.-S. Chu, K.-K. Tian, Y.-H. Zhang, W.-G.g Bi, Z.-H. Zhang, and H.-C. Kuo, "On the Carrier Transport for InGaN/GaN Core-Shell Nanorod Green Light-emitting diodes," IEEE Transactions on Nanotechnology, vol. 18, pp. 176-182, 2018.
9. Z.-H. Zhang, J.-Q. Kou, **Sung-Wen Huang Chen**, H. Shao, J.-M. Che, C.-S. Chu, K.-K. Tian, Y.-H. Zhang, W.-G. Bi, and H.-C. Kuo, "Increasing the hole energy by grading the alloy composition of the p-type electron blocking layer for very high-performance deep ultraviolet light-emitting diodes," Photonics Research, vol. 7, no. 4, pp. B1-B6, 2019.

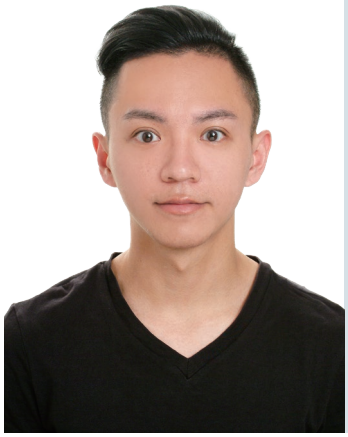
指導教授

郭浩中 講座教授

現職　國立交通大學 / 光電工程學系

學歷　美國伊利諾大學厄巴納香檳分校 / 電機與計算機工程學系博士

經歷　・國立交通大學 / 特聘、講座教授 (2013 ~ now)
・美國加州大學柏克萊分校 / 訪問學者 (2018 ~ 2019)
・台積固態照明 / 研發處長 (2011 ~ 2013)
・ IEEE, OSA, SPIE, IET Fellow



周川普 Chuan-Pu Chou

國立清華大學 工程與系統科學系

獲獎摘要

周川普同學 2016 年自國立台灣師範大學碩士班畢業後即以優異的成績進入清華大學工程與系統科學系就讀博士班。研究領域為改接觸電阻 (Contact Resistivity Improvement)、多晶鍺錫化合物應用於積層式 3D-IC (Poly-GeSn Devices Apply for Monolithic 3D-IC) 及類神經型態運算 (Neuromorphic Computing)。曾參與 Silicon Nanoelectronics Workshop (SNW)、IEEE Semiconductor Interface Specialists Conference (SISC) 及 Insulating Films on Semiconductors (INFOS) 等國際會議。

得獎經歷

- 2019 年財團法人中技社科技研究獎學金
- 2018 台積電研究助理獎學金
- 2017 台積電研究助理獎學金

重要學術著作與專利

1. **Chuan-Pu Chou**, Chin-Yu Chen, Kuen-Yi Chen, Shih-Chieh Teng, Jia-Hong Huang, and Yung-Hsien Wu, “Improved Current Drivability for Sub-20-nm Contact With Reverse Retrograde Profile”, IEEE Electron Device Letters, vol. 38, no. 3, pp. 299-302, 2017.
2. **Chuan-Pu Chou**, Chin-Yu Chen, Kuen-Yi Chen, Shih-Chieh Teng, Yung-Hsien Wu, “Improved leakage current and device uniformity for sub-20 nm N-FinFETs by cryogenic Ge pre-amorphization implant in contact”, Microelectronic Engineering, vol. 178, pp.137-140, 2017.
3. **Chuan-Pu Chou**, Hui-Hsin Chang, and Yung-Hsien Wu, “Enabling Low Contact Resistivity on n-Ge by Implantation After Ti Germanide”, IEEE Electron device letters, vol. 391, no.1, pp. 91-94, 2018. (Impact factor: 4.221, for Engineering, Electrical & Electronic, 2019 JCR Report).
4. **Chuan-Pu Chou**, Yan-Xiao Lin, and Yung-Hsien Wu, “Implementing P-Channel Junctionless Thin-Film Transistor on Poly-$Ge_{0.95}Sn_{0.05}$ Film Formed by Amorphous GeSn Deposition and Annealing”, IEEE Electron device letters, vol. 39, no. 8, pp. 1187-1190, 2018.
5. **Chuan-Pu Chou**, Yan-Xiao Lin, Kuan-Ying Hsieh and Yung-Hsien Wu, “Poly-GeSn junctionless P-TFTs featuring a record high I_{ON}/I_{OFF} ratio and hole mobility by defect engineering”, Journal of Materials Chemistry C, vol. 7, no. 17, pp. 5201-5208, 2019.
6. **Chuan-Pu Chou**, Yan-Xiao Lin, Kuan-Ying Hsieh and Yung-Hsien Wu, “Investigation of Capping Layer on Characteristics of Poly-GeSn Junctionless p-Channel Thin Film Transistors”, ECS Journal of Solid State Science and Technology, vol. 8, no. 11, pp. P647-P651, 2019.
7. **Chuan-Pu Chou**, Yan-Xiao Lin, Yu-Kai Huang, Chih-Yu Chan, and Yung-Hsien Wu, “Junctionless Poly-GeSn Ferroelectric Thin-Film Transistors with Improved Reliability by Interface Engineering for Neuromorphic Computing”, ACS Appl. Mater. Interfaces, vol. 12, no. 1, pp. 1014-1023, 2020.
8. **Chuan-Pu Chou**, Yan-Xiao Lin, Yu-Kai Huang, Chih-Yu Chan, and Yung-Hsien Wu, “Impact of GeSn Crystallinity on Reliability of Ferroelectric HfZrOx for Devices with Metal-Ferroelectric-Semiconductor Structure”, Phys. Status Solidi Rapid Res. Lett., 2020.
9. **Chuan-Pu Chou**, Yan-Xiao Lin, and Yung-Hsien Wu, “Dependence of capping layer and annealing ambient on quality of poly-GeSn film and performance of p-channel junctionless thin film transistor”, Silicon Nanoelectronics Workshop, 2018.
10. **Chuan-Pu Chou**, Yan-Xiao Lin, Yu-Kai Huang, Chih-Yu Chan, and Yung-Hsien Wu, “Dependence of Reliability of Ferroelectric HfZrOx Thin Film on Poly- and Single Crystalline-GeSn by solid phase epitaxy on Si(100) and Si(111) Wafer”, in IEEE Semiconductor Interface Specialists Conference, 2019.

指導教授

巫勇賢 教授

現職　國立清華大學 / 工程與系統科學系

學歷　・國立清華大學 / 電機工程學士
　　・國立交通大學 / 電子工程學系博士

經歷　・國立清華大學 / 副學務長
　　・國立清華大學 / 推廣教育主任
　　・國立清華大學 / 原子科學院學士班主任
　　・ IET Fellow / IEEE Senior Member

林家君 Chia-Chun Lin

國立清華大學 資訊工程學系

獲獎摘要

林家君同學自 2016 年起於國立清華大學資訊工程學系攻讀博士班。研究領域為邏輯合成、設計驗證及新興科技的自動化設計，其研究成果已分別發表於 IEEE 期刊以及其他重要國際會議。林同學曾於 2018 年的國際積體電路電腦輔助設計軟體製作競賽獲得冠軍 (CAD contest at ICCAD 2018, First Prize)。除了豐碩的研究成果外，林同學也擔任國立清華大學的兼任講師，並在教學評鑑中獲得修課同學相當高的評價。

得獎經歷

- CAD contest at ICCAD 2018, First Prize
- Ministry of Education 2017 IC / CAD Contest, Second Prize

重要學術著作

1. **Chia-Chun Lin**, Hsin-Ping Yen, Sheng-Hsiu Wei, Pei-Pei Chen, Yung-Chih Chen, and Chun-Yao Wang, "A General Equivalence Checking Framework for Multivalued Logic", IEEE Asia and South Pacific Design Automation Conference, 2021.
2. **Chia-Chun Lin**, Chin-Heng Liu , Yung-Chih Chen, and Chun-Yao Wang, "A New Necessary Condition for Threshold Function Identification", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020.
3. **Chia-Chun Lin**, Kit Seng Tam, Chang-Cheng Ko, Hsin-Ping Yen, Sheng-Hsiu Wei, Yung-Chih Chen, and Chun-Yao Wang, "A Dynamic Expansion Order Algorithm for the SAT-based Minimization", IEEE International System-on-Chip Conference, 2020.
4. Hsiao-Yu Chiang, Yung-Chih Chen, De-Xuan Ji, Xiang-Min Yang, **Chia-Chun Lin**, and Chun-Yao Wang, "LOOPLock : LOgic OPtimization based Cyclic Logic Locking", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020.
5. Ya-Chun Chang, **Chia-Chun Lin**, Yi-Ting Lin, Yung-Chih Chen, and Chun-Yao Wang, "A Convolutional Result Sharing Approach for Binarized Neural Network Inference", IEEE Design Automation and Test in Europe, 2020.
6. Chin-Heng Liu, **Chia-Chun Lin**, Yung-Chih Chen, Chia-Cheng Wu, Chun-Yao Wang, and Shigeru Yamashita, "Threshold Function Identification by Redundancy Removal and Comprehensive Weight Assignments", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019.
7. Hsin-Pei Wang, **Chia-Chun Lin**, Chia-Cheng Wu, Yung-Chih Chen, and Chun-Yao Wang, "On Synthesizing Memristor-Based Logic Circuits with Minimal Operational Pulses", IEEE Transactions on Very Large Scale Integration Systems, 2018.
8. Yung-An Lai, **Chia-Chun Lin**, Chia-Cheng Wu, Yung-Chih Chen, and Chun-Yao Wang, " Efficient Synthesis of Approximate Threshold Logic Circuits with an Error Rate Guarantee", IEEE Design Automation and Test in Europe, 2018.
9. **Chia-Chun Lin**, Chiao-Wei Huang, Chun-Yao Wang, and Yung-Chih Chen, " In&Out: Restructuring for Threshold Logic Network Optimization", IEEE International Symposium on Quality Electronic Design, 2017.
10. **Chia-Chun Lin**, Chun-Yao Wang, Yung-Chih Chen, and Ching-Yi Huang, " Rewiring for Threshold Logic Circuit Minimization" , IEEE Design Automation and Test in Europe, 2014.

指導教授

王俊堯 特聘教授

現職　國立清華大學 / 資訊工程學系

學歷　國立交通大學 / 電子工程學系博士

經歷
- 國立清華大學 / 計算機與通訊中心主任 (2019 ~ present)
- 國立清華大學 / 教育部實踐研究計畫工程學門副召集人 (2019 ~ present)
- 國立清華大學 / 電機資訊學院學士班系主任 (2015 ~ 2019)
- 美國伊利偌大學 / 香檳分校訪問學者 (2014)
- 美國賓州州立大學 / 訪問學者 (2010)

TSIA 2020 半導體獎

博 士 研 究 生

徐子翔 Tzu-Hsiang Hsu

國立清華大學 電機工程學系

獲獎摘要

徐子翔同學自 2016 年起於國立清華大學電機工程學系 - 系統組攻讀博士班。主要研究領域為結合人工智慧與客製化應用之影像感測器 (CMOS Image Sensor)，其包含低電壓與低功耗電路設計、感測器內運算 (Processing-in-Sensor) 電路設計。研究成果曾於 ISSCC、VLSI-Symp.、IEDM、ASSCC 等 IEEE 頂尖國際會議發表。

得獎經歷

- 2020 年 TSRI 台灣半導體研究中心優良晶片設計獎 - 特別設計獎 / 特優設計獎
- 2020 年財團法人聯詠科技教育基金會獎學金
- 2019 年 IEEE 亞洲固態電路研討會 ASSCC-2019 Highlighted Paper and Best Student Design Award
- 2019 年 TSRI 台灣半導體研究中心優良晶片設計獎 - 優等設計獎
- 2015 年國立清華大學 - 梅貽琦獎章
- 2012 ~ 2019 年全國大專校院運動會一般男子組游泳項目共獲獎牌 20 金 4 銀 13 銅

重要學術著作

1. **T.-H. Hsu***, Y.-K. Chen*, and C.-C. Hsieh et al., "A 0.8V Multimode Vision Sensor for Motion and Saliency Detection with Ping-Pong PWM Pixel," 2020 IEEE International Solid-State Circuits Conference (ISSCC), pp. 110-112, Feb. 2020. (Speaker)
2. **T.-H. Hsu** and C.-C. Hsieh et al., "A 0.5V Real-time Computational CMOS Image Sensor with Programmable Kernel for Always-on Feature Extraction," 2019 IEEE Asian Solid-State Circuits Conference (ASSCC), pp. 33-34, Nov. 2019. (Speaker)
3. **T.-H. Hsu** and C.-C. Hsieh et al., "AI Edge Devices Using Computing-In-Memory and Processing-In-Sensor: From System to Device" 2019 IEEE International Electron Devices Meeting (IEDM), pp. 22.5.1-22.5.4, Dec. 2019. (Invited)
4. K.-T. Tang, …**T.-H. Hsu**, …C.-C. Hsieh and M.-F. Chang, "Considerations of Integrating Computing-In-Memory and Processing-In-Sensor into Convolutional Neural Network Accelerators for Low-Power Edge Devices," 2019 IEEE Symposia on VLSI Circuits (VLSI-Symp.), pp. T166-T167, Jun. 2019.
5. **T.-H. Hsu**, T. Liao, N.-A. Lee, and C.-C. Hsieh, "A CMOS Time-of-Flight Depth Image Sensor With In-Pixel Background Light Cancellation and Phase Shifting Readout Technique," IEEE Journal of Solid-State Circuits (JSSC), vol 53, no. 10, pp. 2898-2905, Oct. 2018.
6. W.-H. Chen, …**T.-H. Hsu**, …C.-C. Hsieh, K-T. Tang, M-F. Chang, "A 65nm 1Mb Nonvolatile Computing-in-Memory ReRAM Macro with Sub-16ns Multiply-and-Accumulate for Binary DNN AI Edge Processors," 2018 International Solid-State Circuits Conference (ISSCC), pp. 494-495, Feb. 2018.
7. H.-L. Chen, S.-E. Hsieh, **T.-H. Hsu**, C.-C. Hsieh, "A CMOS Imager for Reflective Pulse Oximeter with Motion Artifact and Ambient Interferer Rejections," 2018 IEEE Asian Solid-State Circuits Conference (ASSCC), pp. 25-26, Nov. 2018. (Speaker)
8. **T.-H. Hsu**, and C.-C. Hsieh, "A CMOS Imaging Platform Using Single Photon Avalanche Diode Array in Standard Technology," in IEEE Sensors Conference, pp. 1-3, Oct. 2017. (Speaker)

指導教授

謝志成 教授

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學歷　國立交通大學 / 電子工程學系博士

經歷
- PixArt Imaging Inc., Taiwan (1999 ~ 2007)
- IEEE Solid-State Circuit Letter (SSCL), Associate Editor (2017~)
- IEEE Circuits and Systems Magazine (CASM), Associate Editor (2020~)
- IEEE SSCS Taipei Chapter, Chair (2019)
- ISSCC/A-SSCC, Technical Program Committee (TPC)

陳宏誌 Hong-Chih Chen

國立成功大學 光電工程研究所

獲獎摘要

陳宏誌同學自 2016 年起於國立成功大學光電工程研究所攻讀博士班。研究領域為薄膜電晶體 (Thin-Film Transistors, TFTs)、高電子遷移率晶體管 (High-Electron-Mobility Transistors, HEMTs)、金屬氧化物半導體場效電晶體 (Metal-Oxide-Semiconductor Field-Effect Transistors, MOSFETs)、記憶體 (Memory)，主要釐清各種元件電性和可靠度異常，並提出相應解決方案。陳宏誌同學研究成果豐碩在 SCI 國際期刊刊登了第一作者篇數 11 篇 (IEEE Electron Device Letters 5 篇、IEEE Transactions on Electron Devices 4 篇、ACS applied materials & interface 2 篇) 於頂尖國際期刊中提出電子元件相關研究。

重要學術著作

1. **Hong-Chih Chen**, Shin-Ping Huang, Yu-Fa Tu, Chuan-Wei Kuo, Kuan-Ju Zhou, Jian-Jie Chen, Yu-Shan Shih, Guan-Fu Chen, Wan-Ching Su, Hong-Yi Tu, Hui-Chun Huang, Wei-Chih Lai and Ting-Chang Chang, Inhibiting the Kink Effect and Hot-carrier Stress Degradation using Dual-gate Low-temperature Poly-Si TFTs, IEEE Electron Device Letters, vol. 41, no.1, pp. 54–57. Nov. 2019. DOI: 10.1109/LED.2019.2951935 (IF=4.2)
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獲獎摘要

曹俞慶同學自 2016 年起於國立中山大學物理所攻讀博士班，博士班期間專注研究薄膜電晶體 (Thin Film Transistor) 與氮化鎵功率元件 (GaN High Electron Mobility Transistor)。薄膜電晶體部分，對於主動層材料為非晶銦鎵鋅氧 (a-IGZO) 與多晶矽 (Low Temperature Poly-Silicon) 的元件深入探討其在照光下的不穩定性 (Negative Bias Illumination Stress)，大電流下操作的可靠度問題 (Self-heating Stress) 與相關的物理機制。氮化鎵功率元件部分，藉由設計元件保護層材料的介電常數，改變元件內部電場分布，有效提升元件的崩潰電壓。這些研究成果共發表 6 篇國際期刊與 1 項台灣專利與 1 項美國專利 (4 項台美專利申請中)。

得獎經歷

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黃馨平同學自 2016 年起於國立中山大學光電工程研究所攻讀博士班，博士班期間專注研究多晶矽 (Low Temperature Poly-Silicon) 薄膜電晶體 (Thin Film Transistor)，深入探討其在 DC 及 AC 操作下的不穩定性、大電流下操作的可靠度問題 (Self-heating Stress) 與相關的物理機制。這些研究成果共發表至 5 篇國際期刊，分別發表於 IEEE EDL (3 篇)、IEEE TED (2 篇) ，1 項台灣專利申請中；曾於 2019 年 IEEE IEDM 頂尖國際會議中發表一種新穎結構可有效提升可撓式電晶體於彎曲下之可靠度相關研究。馨平在學習領域成果豐碩，難能可貴。

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